Center for Advanced Power Systems
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Testing the Megawatt-Scale Impedance Measurement Unit at Medium Voltage Levels

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Executive Summary

The Office of Naval Research is developing science and technology for advanced electric ships that utilize an integrated power system. This project was motivated by the success and feasibility of impedance measurements and impedance-based controls at the low voltage level. An extension of impedance measurement units (IMU) to the medium voltage (MV), megawatt-class converter levels would provide significant benefits to the U.S. Navy. The primary objective of this project was to evaluate the suitability of such a novel instrument for use of frequency domain characterization of megawatt scale equipment, which will eventually be used for system integration studies. This project was the first test and use of an IMU at these voltage and power levels, following the design and preliminary testing of the MV IMU. The technical objectives included demonstration of the IMU design concept and impedance measurement capabilities within both AC- and DC-systems.

The testing approach was derived in coordination between the Center for Advanced Power Systems (CAPS) at Florida State University and the Center for Power Electronics Systems (CPES) at Virginia Tech. The IMU's power stage design is based on the PEBB (Power Electronic Building Block) concept, and individual stages were evaluated before operating the unit as an impedance measurement device. Test applications feasible at CAPS concerned 3.3 kV/60 Hz, and 4.16 kV/60 Hz, and 4 kV DC-systems. Guided by modeling and simulation efforts in the related ESRDC Impedance-based Controls task, commissioning and test plans were established. The pre-testing work addressed issues of experiment selection and design. One critical aspect was the protection of experiments due to the uniqueness of the proposed tests. The system-based tests were conducted with the help of a Real Time Simulator (RTS) to facilitate Control Hardware-in-the-Loop simulations and control of the surrounding power system components.

Benefits and successful outcomes of the project includes the following: Test procedures and protection logic and actions could be implemented with the help of representative models within the RTS platform, supporting verification and validation of experiment design and protection. The medium voltage, megawatt-level facilities at CAPS provided several means of subjecting the device under test to realistic surrounding system conditions, and both AC- and DC-configurations could be evaluated. Impedances characteristics were successfully determined by the IMU at the medium voltage level.

The most challenging problems experienced during testing are related to the SiC-modules and common mode issues. These issues were to some extend expected due to the high switching frequency and partly mitigated by the initial design itself. Additional measures were taken while testing was progressing from low to medium voltage levels.

The project did not achieve the target voltage levels of 4.16 kV_{AC} but operated at 2.8 kV_{AC} in both shunt and series mode instead. The project team suggests the following two research items as best options to move forward and improve IMU capabilities at the MV-level: improve switching characteristics of SiC-modules with respect to shoot-through and reduce common mode sensitivity. The first part will need to improve the design of the integrated SiC- and firing pulse circuits. The second part will require establishing design guidelines on both IMU-device and system level.

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Terminology and Acronyms

AC	alternating current
CAPS	Center for Advanced Power Systems
CHIL	Controller Hardware-in-the-Loop
CPES	Center for Power Electronics Systems
DAQ	data acquisition system
RTDS	Real Time Digital Simulator® from RTDS Technologies, Inc.
DUT	device under test
DC	direct current
FSU	Florida State University
IMU	Impedance measurement unit
JBS	Junction barrier Schottky
PHIL	power hardware-in-the-loop
pu	per unit
rms	root mean square
RoS	rest–of-system
RTS	real-time simulator
SiC	Silicon carbide
VT	Virginia Tech

1 Introduction

The stability of converters and converter-based power distribution systems can be evaluated with the help of impedance characterization, which provides a means to predict the effect of converter interactions in medium voltage systems. Several impedance-based stability criteria have been proposed in the literature, starting from the Middlebrook Criterion and continuing with criteria proposed by the Electric Ship Research and Development Consortium (ESRDC) researchers, such as the root exponential stability criterion (RESC, [1]) and the passivity-based stability criterion [2]. Extensions to AC-systems have been addressed in [3] by part of the Center for Power Electronics Systems (CPES) project team members. Additionally, online impedance monitoring provides the possibility of system state monitoring and control adaptation to ensure control robustness without sacrificing performance. These techniques have great Navy relevance, because the electric-ship power distribution system consists of a network of interconnected feedback-controlled switching converters and is subject to converter interactions and potential instability.

Currently, no commercial products exist that are adequate to measure impedance at the medium voltage application level. The efforts reported herein encompassed modeling and simulation to determine efficient means of designing, operating, and protecting test setups, laboratory experiments, and result analysis. The IMU-research challenges identified were: (i) determining the inherent noise level in voltages and currents measured within converter-dominated systems, (ii) selecting the injection signal pattern, (iii) evaluating resolution and dynamic characteristics required from voltage and current probes, (iv) developing a robust algorithm for impedance computations, (v) demonstrating a low-risk prototype implementation, and (vi) demonstrating impedance characterization in a medium voltage facility.

The Center for Power Electronics Systems at Virginia Tech developed and built a medium voltage class impedance measurement unit (IMU, [4]), targeting applications which require measuring the input and output impedances of power systems at kV and MW levels (both DC and three-phase AC). The advanced power test facility at FSU-CAPS provides one of the most suitable test-sites for IMU deployment. Additionally, although CPES has already addressed the research challenges mentioned above (specifically i, ii, iv and v) through the low-voltage IMU development and demonstration project done for Newport News Shipbuilding in 2012 [5][6], the results obtained for (i) and (ii) have not been fully validated, and were not performed at the medium-voltage level. This joint project allowed to design and execute experiments that explore the IMU's full capabilities for both medium voltage alternating current (MVAC) and direct current (MVDC) applications.

The following sections report on the project tasks including test setups and scenarios, model building and Controller Hardware-in-the-Loop simulation, and impedance measurement results. Furthermore, a section on specific observations made while testing is included.

2 Medium Voltage Test Facility

The following summarizes the medium voltage and megawatt-level test facility available for the tests at CAPS. The two key test facilities available are the Variable Voltage Source (VVS), and the Modular Multi-level Converter (MMC). An overview the facilities including the VVS and MMC is shown in Figure 1, see also Table 2 in Appendix A for technical data. The VVS nominally provide 0-4.16 kV/5 MW at a frequency range of about 45-75 Hz. The VVS can further be split into an AC and a DC system, allowing to also operate with 0-1.15 kV_{DC}/2.5 MW. Each of the four MMCs is rated for 0-6 kV, 210 A, 1.25 MW, and the converters can be flexibly operated in parallel, series, or back-to-back. Additionally, the MMCs can be supplied from the VVS at nominally 3.3 kV, 60 Hz. A list of equipment used in given in Appendix A, Table 2.

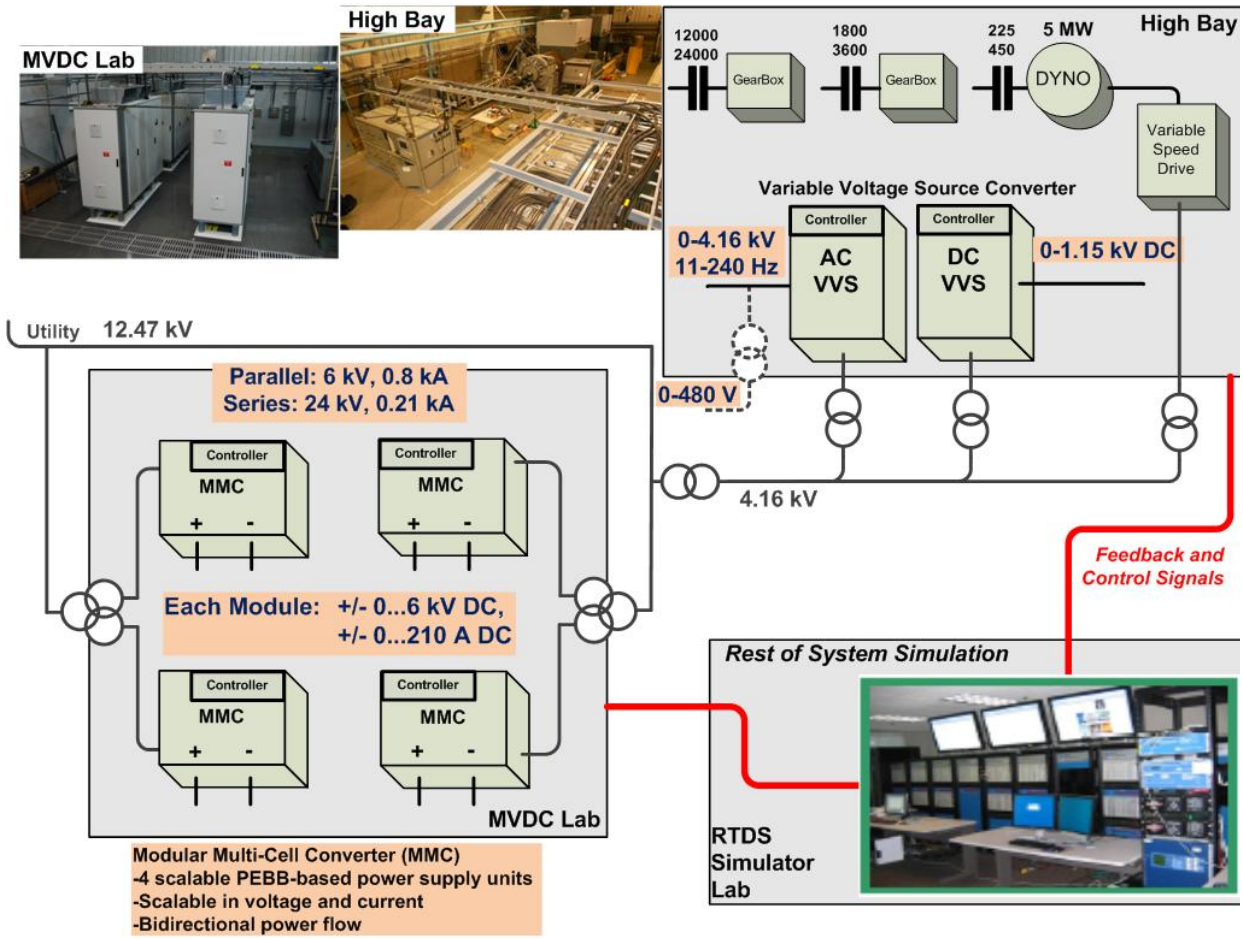


Figure 1. Overview of the medium voltage megawatt-level test facility

One of main feature of the test facility is the capability to operate and control both the VVS and the MMCs through a real time simulator (RTS): a 14-rack digital real-time simulator from RTDS Technologies. In the experiments reported herein, the RTS was used to control the surrounding system, also referred to Rest-of-System (RoS), as seen by the IMU.

The VVS and MMC allow the IMU to be operated within AC- and DC-system setups, and the corresponding details are provided in the test setups section below.

3 Impedance Measurement Unit

Characteristics of the impedance measurement unit are as follows. The IMU is based on three Power Electronic Building Block (PEBB) subsystems, see Figure 2. Each PEBB uses an H-bridge with SiC MOSFET modules (PEBB 6000 beta prototypes), an internal DC-bus with capacitors, and protection circuits. The IMU unit includes interconnection terminals to facilitate operation in AC- and DC-systems in both shunt and series mode.

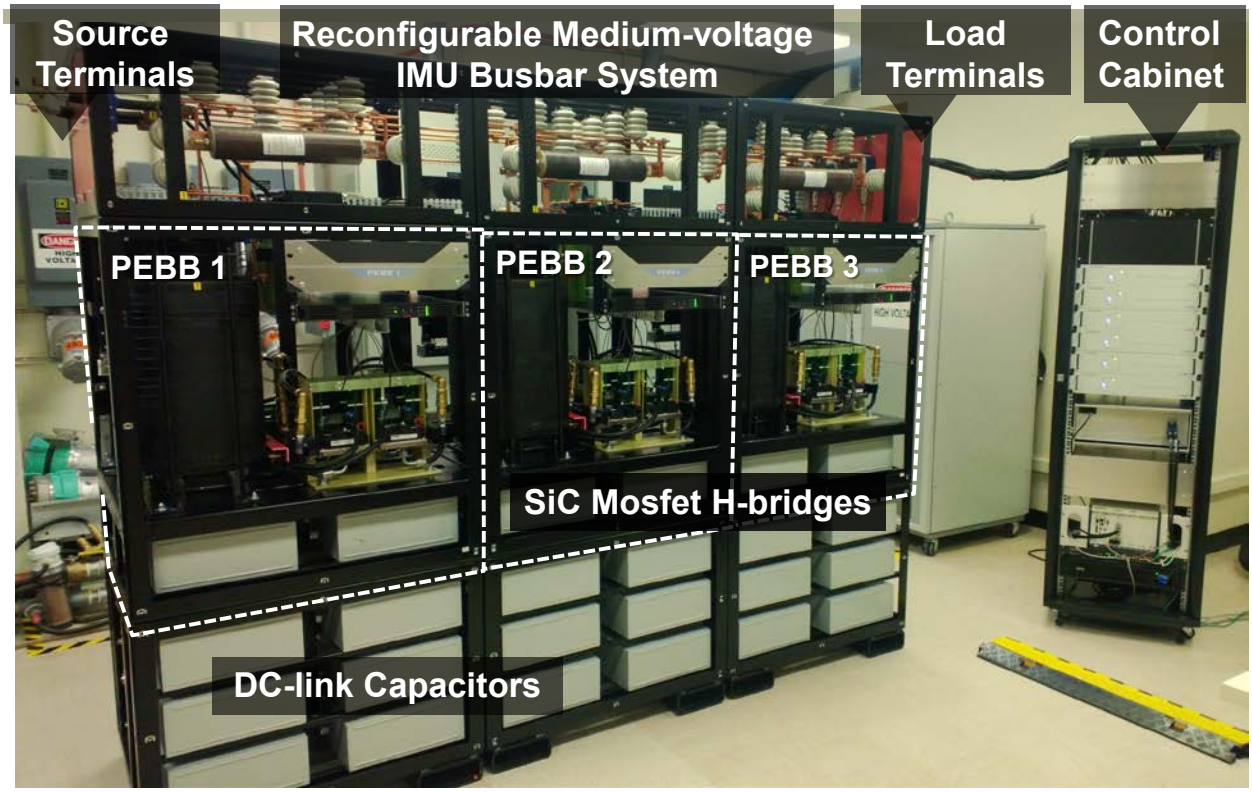


Figure 2. Impedance Measurement Unit

With respect to AC systems, the nominal system frequency can range from 60 Hz to 400 Hz, the nominal voltage level is 4.16 kV, and nominal system current level is 300 A. For DC-system operation, the nominal voltage and current level are 6 kV and 300 A, respectively. See also Appendix B, Table 3 for a list of specifications.

4 Test Setups

This section provides an overview of the test setups selected. The test setups were partly identified and selected after detailed, offline simulations had been performed to predict feasibility and operating conditions. The setups are listed in Table 1. The table also provides information on the outcomes. As not all setups could be successfully tested to the full rated values, the highest achieved voltage levels are given.

Table 1. List of IMU Test Setups

Setup	Objective	Description and Purpose	Outcome
C1	Commissioning	Double-pulse test of IGBT modules, a repeat of tests performed at CPES-VT to confirm functional components and IMU installation at CAPS.	**Successful**
C2	Commissioning: DC filter test	Testing operation from MMCs using PEBB filter (R-C) and inductive filter between PEBB and MMC unit.	Successful once common mode currents were alleviated by grounding DC-bus midpoint
C3	Commissioning: PEBB buck mode setup	Operating PEBB leg as buck converter, one MMC as DC voltage source.	Highest voltage levels achieved: 4kV, 2 kV, and 3 kV for the three PEBBs, respectively.
1	PEBB power stage testing (buck mode)	Heat run (power testing) of single PEBB units. Each of the three IMU-PEBB units to demonstrate full voltage and current capabilities. PEBB (with internal capacitor) is connected to an MMC on the DC-bus side and controlling the current into resistive load.	**Highest achieved: 4kV, 15% modulation, ~100 kVA, 30 minutes**
2	AC impedance measurement (low voltage)	Using VVS-AC and wye-connected resistive load. And a step-down transformer to test at low voltages (480 V).	**Successful**
3	AC impedance measurements (medium voltage)	Using VVS-AC as source with resistive load to allow testing at medium voltages of up to about 2 kV.	**Successful at 1.8 kVac**
4	AC impedance measurements (medium voltage)	Using VVS-AC as source without resistive load to allow testing at medium voltages of up to 4.16 kV, shunt mode.	**Best achieved: 2.8 kVac**
5	AC impedance measurements (medium voltage)	Added AC HIL interface and real-time generator (2.5 kV and 4.875 MVA) to setup #4.	**Successful.**
6	AC impedance measurements (medium voltage)	IMU connected between VVS-AC (source) and AC-input of one MMC transformer, load on low-voltage side, IMU on 4.16 kV side. Series mode operation.	**Best achieved: 2.8 kVac**
7	DC impedance measurements	IMU connected between MMCs on DC-bus. Four MMCs are available to operate in various arrangements. For example, two MMCs as sources and one MMC as load. Demonstration of MVDC impedance measurement capabilities.	not performed

5 PEBB and IMU Testing

The following provides a chronological list of IMU-related tests as progressing through commissioning, power stage tests, and impedance measuring. Not included are tests and events that were related to configuring and verifying the real time simulator cases and data acquisition. In the following DUT refers either to a PEBB module or the IMU as a whole.

1. Double-pulse tests of all 6 switching modules in the IMU performed
    a. Both top and bottom switches tested successfully.
2. PEBB module 1 testing, single leg buck mode – 30% duty cycle, 32 ohm load – MVDC/MMC ungrounded (see Figure 3)
    a. 0.5 kV, 1.0 kV, 1.5 kV, 2.0 kV, 2.5 kV, 3 kV, 3.5 kV (successful)
    b. 4.0 kV – DUT tripped (non-active PEBB units tripped)
    Corrective measure attempted: Protection fibers were removed for PEBBs 2 and 3. Continuing buck mode tests. The control cabinet UPS was unplugged from the wall, and a fiber was replaced, common mode chokes were added to the PEBB 1 UPS power supply cable.
    Outcome: PEBB 1 kept tripping before reaching 1 kV
    Corrective measures attempted: grounding of negative MVDC amplifier rail
    Outcome: DUT tripped while placing MVDC amplifier into standby mode (i.e., switching and controls active at zero output voltage)
    Corrective measure attempted: Using PEBB 3 controller in PEBB 2
    Outcome: Successful operation at 1.5 kV
    Corrective measure attempted: PEBB 1 and 2 operating, PEBB 3 disabled
    Outcome: Successful testing up to 2.5 kV, 10% duty-cycle, trips while ramping to 3 kV supply
3. PEBB H-bridge tests – bulk DC capacitors middle point ungrounded – MVDC/MMC ungrounded
    a. Standby operation and DUT off with 0.5 kV, 1.0 kV, and 2.0 kV successful
4. PEBB H-bridge tests – bulk DC capacitors middle point grounded – MVDC/MMC ungrounded
    a. Standby operation and DUT off with 0.5 kV, 1.0 kV, and 2.0 kV successful
    b. PEBB with 10% modulation and MVDC at 0.5 kV, 1.0 kV, 1.5 kV, 2.0 kV, 2.5 kV, 3.0 kV, 3.5 kV, and 4.0 kV, 4 degree C temperature rise
    c. Trip on transition to 30% modulation
    Corrective measure attempted: modified control code for PWM angle reset
    Outcome: ramping up to and operation at 4.0 kV, 15% modulation for 30 mins (about 100 kVA)
    Additional tests with mid-point ungrounded again resulted in trips at around 1.5 kV. Thus, ground the mid-point and providing a common-mode path seems to be the best setup option.

Adjustments were made on the IMU hardware to reduce susceptibility to common-mode currents: DC-link capacitors were isolated from the frame using non-conductive materials, controls rearranged, and relay discharge wires disconnected. The three PEBB modules now operated more reliably and could be tested with up to 3.5 kV, 2 kV, and 3 kV, respectively.

5. PEBB 1 H-bridge test – bulk DC capacitor middle point ungrounded
    a. 10% modulation with MVDC voltages at 0.5 kV, 1.0 kV, 1.5 kV, 2.0 kV, 3.0 kV, and 3.5 kV; tripped while running 4.0 kV
6. PEBB 2 H-bridge test – bulk DC capacitor middle point ungrounded
    a. 10% modulation with MVDC voltages at 0.5 kV, 1.0 kV, 1.5 kV; tripped while at 2.0 kV

7. PEBB 3 H-bridge test – bulk DC capacitor middle point ungrounded
    a. 10% modulation with MVDC voltages at 0.5 kV -- 2.5 kV; tripped while at 3.0 kV

The system was **reconfigured for IMU shunt operation** between phases A and B. The VVS was operated through a transformer to provide up to 480 V. The wye-connected resistive load bank had a resistance of about 13.6 ohms/phase (see Figure 5).

8. VVS operating at full voltage, providing 480 kVac, IMU DC-link voltages at 800 V
    a. Successfully executed perturbations to measure impedance

9. VVS operating at full voltage, providing 480 kVac, but increasing IMU DC-link voltages
    a. 0.8 kVdc, 1.0 kVdc, 1.2 kVdc, 1.4 kVdc, 1.6 kVdc – DUT tripped

IMU shunt configuration for higher voltages with the AC VVS directly connected (no intermediate transformer) to IMU and WYE connected resistive load bank (13.6 ohms).

10. Increasing AC voltage and IMU DC-link voltages and performing impedance measurements at selected operating points
    a. At 0.48 kVac: 800-1400 V
    b. At 0.80 kVac: 800-1400 V
    c. At 1.0 kVac: 900-1200 V
    d. At 1.5 kVac: 1100 V
    Corrective measure attempted: IMU controls moved away from inductors
    Outcome: Achieved operation at 1.8 kVac

IMU shunt configuration but load bank removed to allow operation at higher AC-voltages.

11. Successful IMU operation at 2.7 kVac measuring source impedance
12. Operation at 3.3 kVac and close to 2 kVdc

Continuing with IMU shunt configuration and testing to **diagnose desaturation trips of IGBT**. In the process some of MOSFET modules were replaced. Bypassing of IGBT in PEBB 3 allowed to increase DC voltage level:

13. Operation at 3.3 kVac and 1.75 kVdc , highest voltage reached was 2.4-2.5 kVdc on IMU DC-bus before tripping

Modified test setup: VVS supplies one of the MMC transformers with load bank in wye-configuration on the low-voltage side. IMU connected on the 4.16 kV side in shunt mode.

14. Operated with up to 3 kVac and 1.4 kVdc before IMU tripped.
    a. Corrective measures attempted: several sensors had to replaced, capacitive filter circuits were added to sensors

The **setup was modified to include an AC HIL interface and generator to the RTS-case**.

15. Testing in AC HIL mode:
    a. Generator set with 2.5 kVac, 4.8 MVA rating: DUT tripped during frequency sweep

b. Modified generator to 1 MVA: tests were halted when interactions/oscillations were noted with the DUT switching

Setup modified for IMU in series mode.

16. Successful IMU operation at 2.8 kV

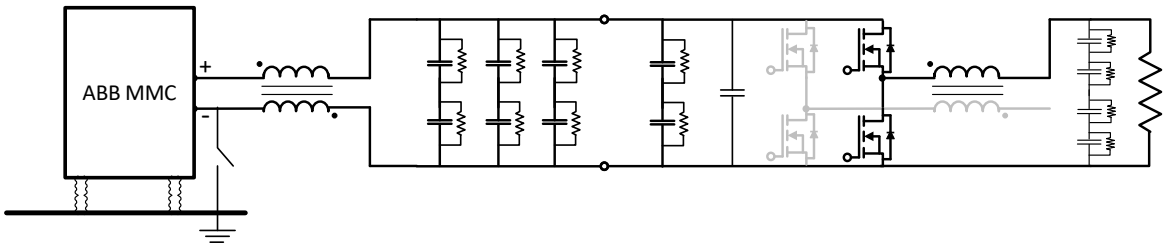


Figure 3. PEBB module testing in buck-mode: Supplied by MVDC with grounding option, input and output filters

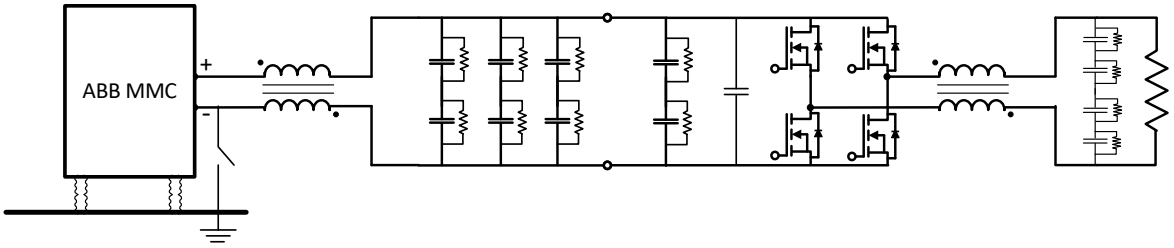


Figure 4. PEBB module testing with H-bridge structure: Supplied by MVDC with grounding option, input and output filters

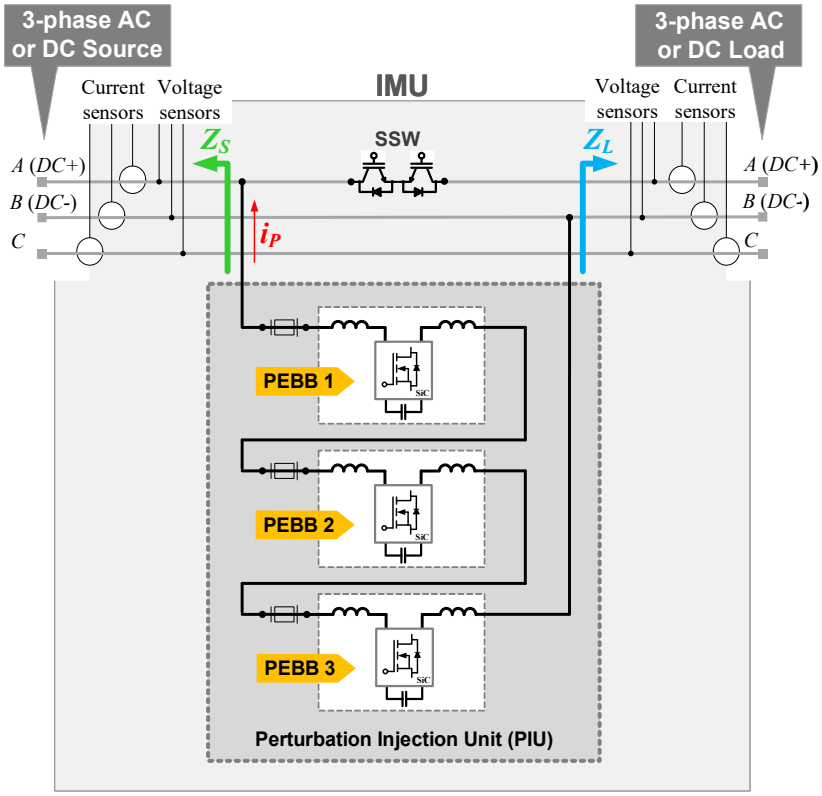


Figure 5. IMU shunt injection mode configuration

6 Discussion

This section provides information on tests performed, test results, difficulties encountered, and steps taken to mitigate problems. The topics addressed in the following are:

- *Double-pulse testing: confirming operational IMU-power stage components;*
- *Buck-mode operation: confirmation of device operation;*
- *Impedance measurement: main testing objective;*
- *Mitigation measures: addressing problems encountered; and*
- *Design improvements: suggestions for future implementations.*

Double-pulse test

The double-pulse test was initially performed at CPES/VT as one of the PEBB-module tests, and provides information on the hard switching characteristics of the individual switching devices. These tests were repeated at CAPS to ensure that transporting and assembling did not cause any problems for the six modules. All tests were successful and confirmed operational SiC-devices (top and bottom switches of a module). An example snapshot of a test at 2 kV and 75 A is shown in Figure 6. The individual traces are: gate signal (yellow, top), current (cyan, 2nd from top, V:I = 1:100), DC voltage (green, 3rd from top), and drain-source voltage (magenta, bottom).

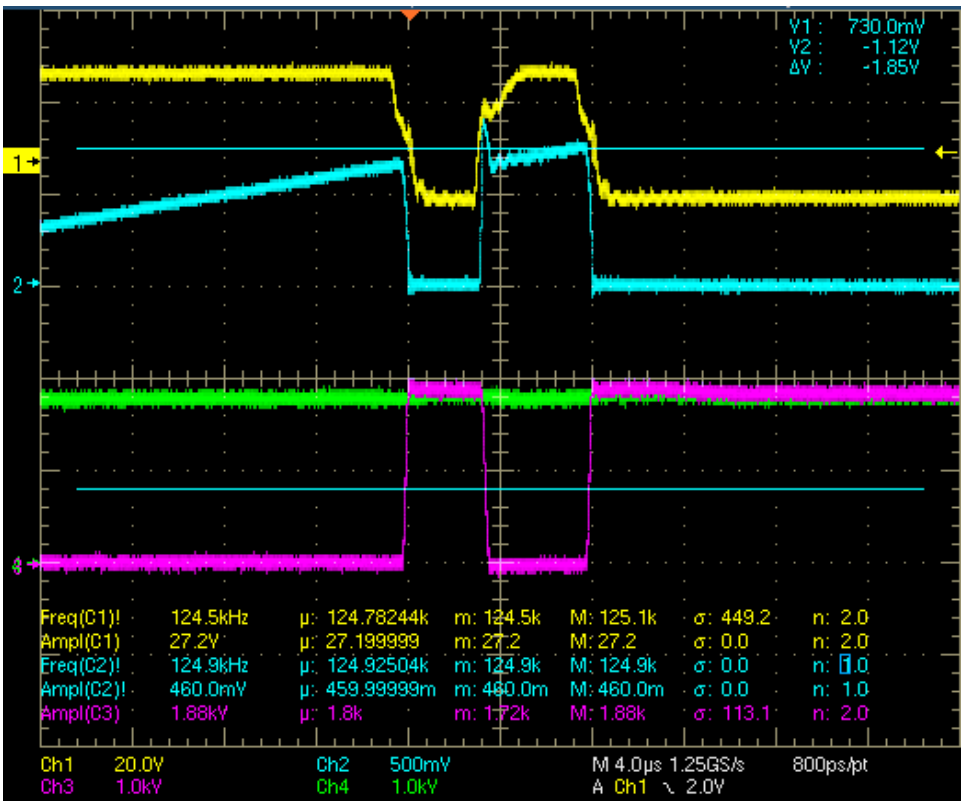
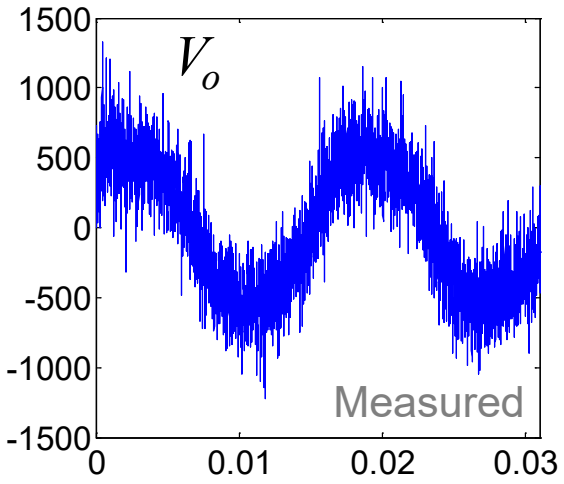


Figure 6. PEBB-Module double pulse test (example capture)

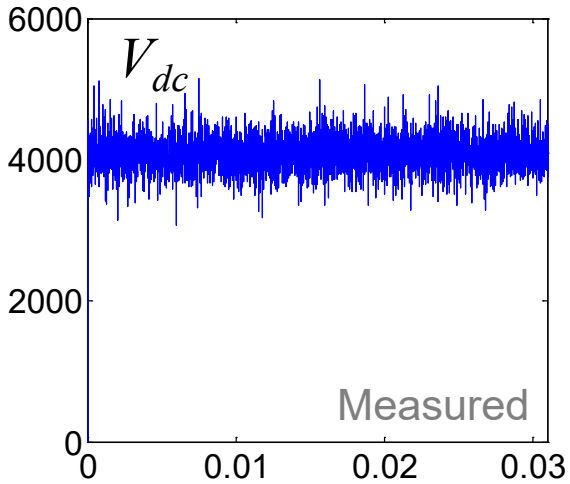
Buck-mode operation

The operation in buck-mode was chosen to confirm the correct operation of a PEBB module (see Figure 3). The MMCs at CAPS were used as a DC source, the upper switch of a module as switching device, the lower device as freewheeling diode, and one of the module inductors as filter. The load was a passive resistive-capacitive circuit.

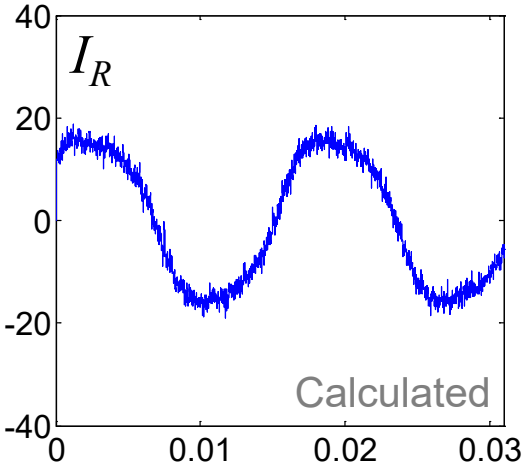
The buck-mode operation was successfully tested up to an input voltage of 2 kV (30% duty cycle, 32 ohm load). Several tests ended with trip events but the recorded fault information reported by the PEBB controllers were inconsistent, i.e., PEBB 1 pointing to an error in PEBB 2, PEBB 2 pointing to an error in PEBB 3, PEBB 3 pointing to an error in PIU controller (high-level controller), etc, with no specific nature of the error. However, the trip voltage-levels were consistent – always around 1.5-2 kV. As only of the three PEBBs was active in this mode, current and voltage sensors of the other two were disconnected but over-current and over-voltage events in these PEBBs kept occurring.



Output voltage (V) vs. time (s)



DC bus voltage (V)



Output current(A) vs. time (s)

Figure 7. Buck-mode operation: voltage and current waveform captures

Experiments were conducted with the MMC ungrounded and one rail grounded but the same tripping symptoms occurred. Also, operating the MMCs in standby mode (i.e., with a DC-voltage of

zero for the buck arrangement) caused intermittent trips. Using one H-bridge, i.e., both PEBB modules, for the buck converter did not make a change the conditions. Changing to a mid-point grounded systems, and therefore providing a path for the common mode currents, did improve the situation and resolved the random tripping events. Typical voltage and current waveforms for the buck mode operation are shown in Figure 7.

Low- and medium voltage Impedance measurements

The IMU was testing in shunt mode as shown in Figure 5 with the VVS in AC-mode and connected through an additional transformer to step-down the voltages to 480 V before connecting to the IMU. The test setup is depicted in Figure 13. A resistive load was used in these tests. Impedances were successfully measured at this voltage level, and the PEBB dc-link voltages were kept balanced to 800 V DC each. The PEBB dc-link voltages were slowly increased in the following tests, but the highest voltages achieved were about 1400 V DC per PEBB (system still 480 V AC with resistive load) before IMU started tripping. An impedance measurement result for a resistive load of 13.8 ohm per phase is shown in Figure 8. Note: the results are depicted with respect to a delta-connected load and, therefore, the values of about 32 dB shown for the main diagonal at low frequency yield wye-connected resistors of $10^{32/20}$ / 3 = 13.3 ohm).

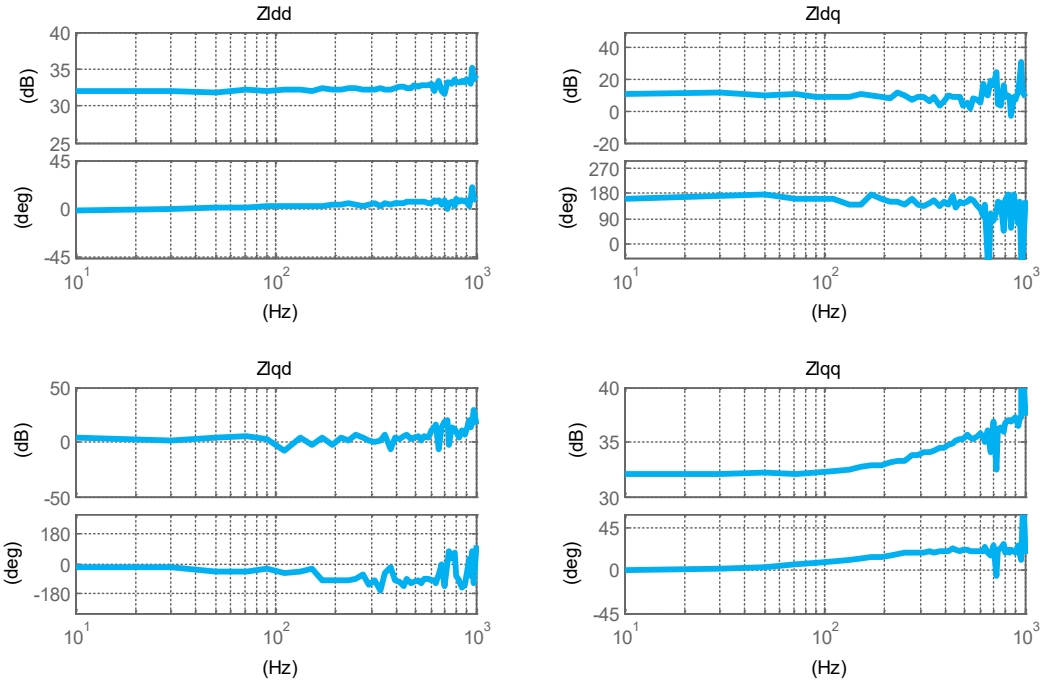


Figure 8. Load impedance measurement result (low voltage, resistive load case)

The impedance measurement tests were repeated for the medium voltage-level using the test setup as depicted in Figure 14. A resistive load bank was connected through a transformer (12.47 kV/3.3 kV) as it is not rated for the medium voltage levels tested here. By slowly raising the AC system voltage through commanding the VVS-AC, the IMU voltage-related capabilities were evaluated. The highest AC-voltages at which the IMU was successfully operated were 2.5 kV and 2.8 kV for the series and shunt mode, respectively. The impedances as determined by the IMU are shown in the following four figures: load impedance via shunt (Figure 9) and series injection

(Figure 10), and source impedance via shunt (Figure 11) and series injection (Figure 12). For example, the measured dd-axis load impedance in the lower frequency range shown in Figure 9 indicates 55 dB, which closely reflects the expected value of 20 $\log_{10}(13.3*3*n^2)$ = 55.1 dB, with n = 12.47/3.3). Note, the resistance in dB reflects the delta-equivalent of the wye-connected 13.3 ohm.

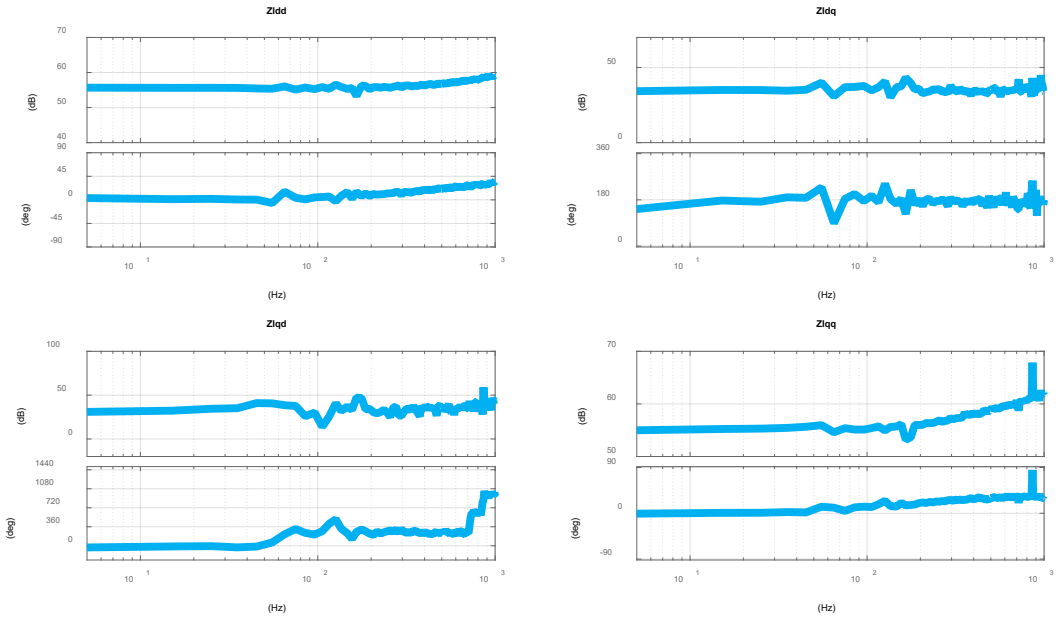


Figure 9. Load impedance measurement result (2.8 kV, resistive load, shunt injection)

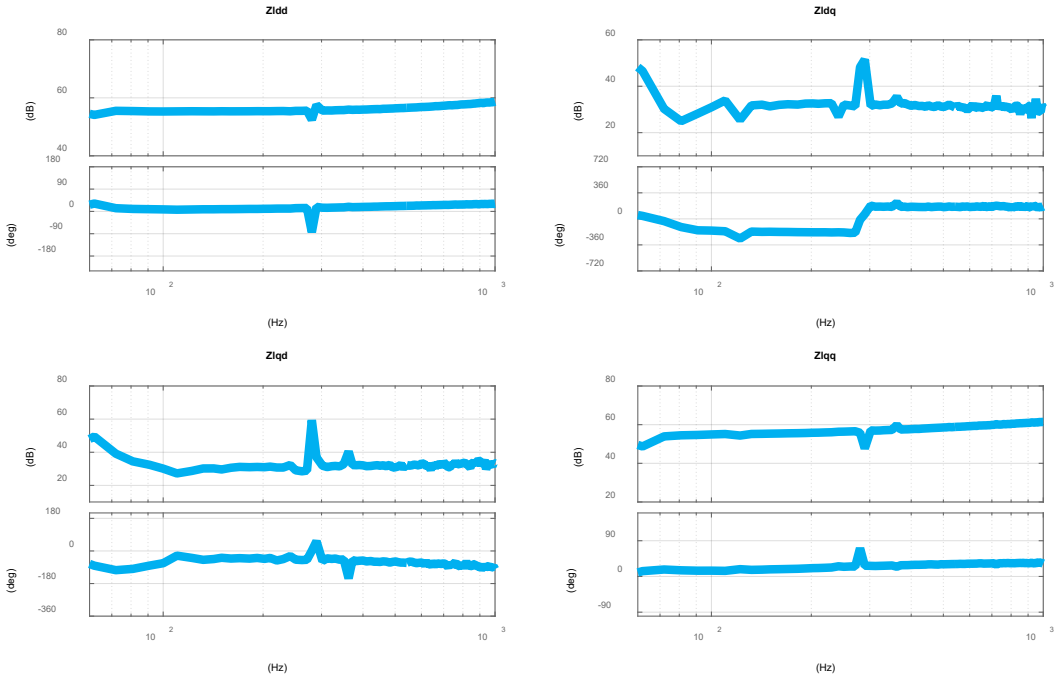


Figure 10. Load impedance measurement result (2.5 kV, resistive load, series injection)

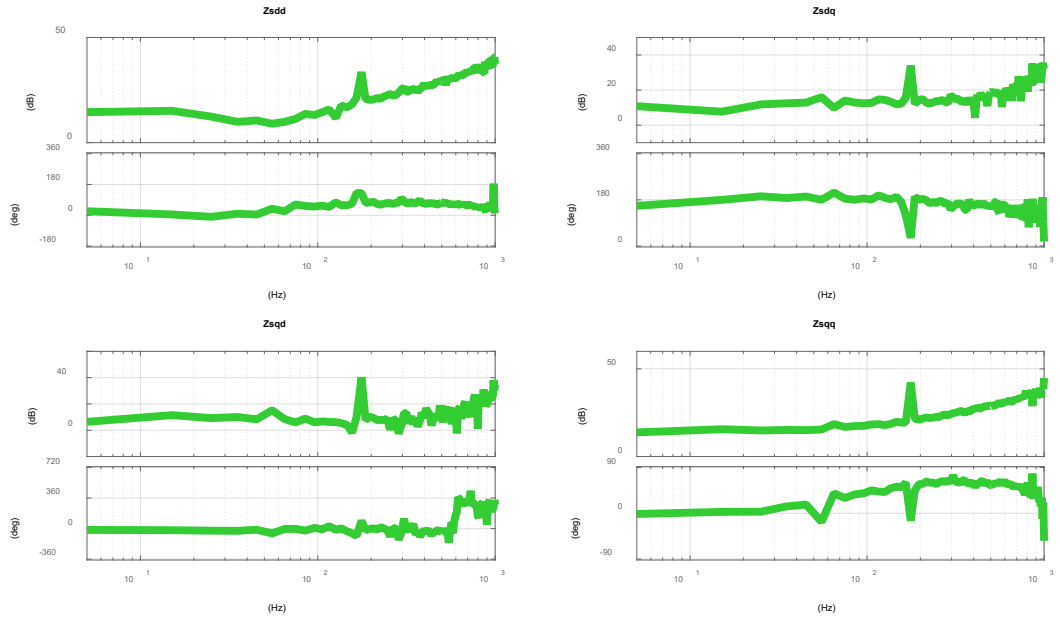


Figure 11. Source impedance measurement result (2.8 kV, resistive load, shunt injection)

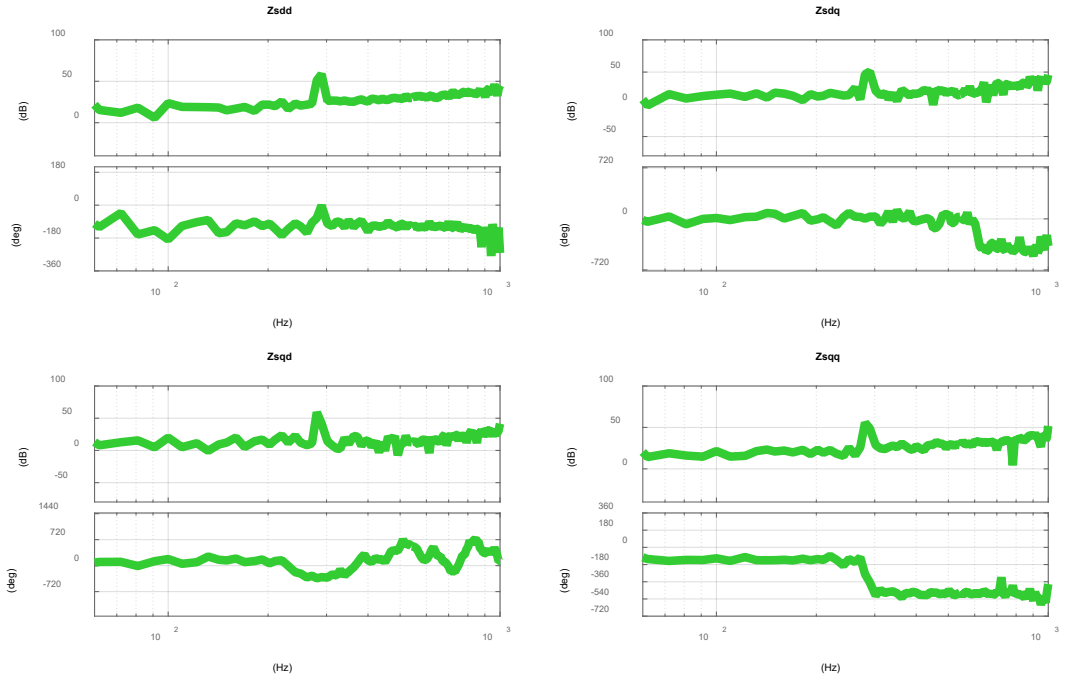


Figure 12. Source impedance measurement result (2.5 kV, resistive load, series injection)

The source impedances as shown in Figure 11 and Figure 12 reflect the characteristics as determined primarily by the controls up to the kHz-range. Afterward the amplifier's interface transformer impedance dominates (see Zsdd in the figures, which increases in magnitude with frequency at an angle approaching 90 degrees leading).

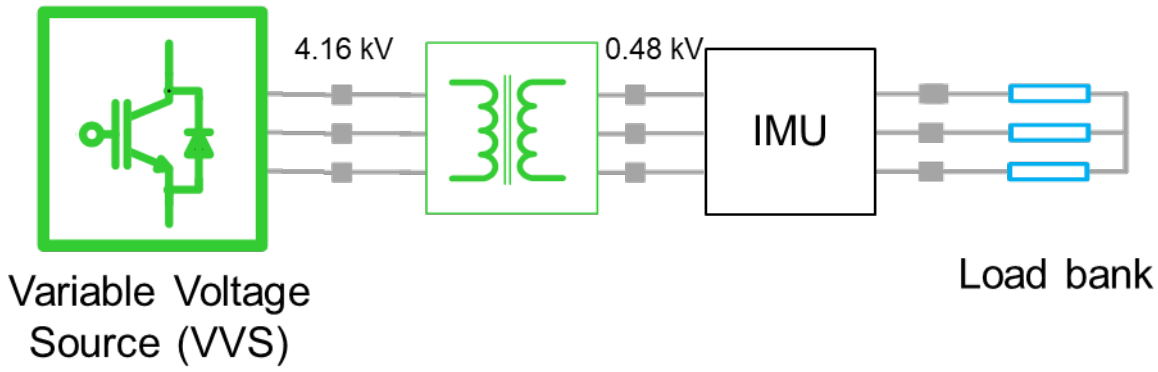


Figure 13. Test setup for low-voltage AC impedance measurement

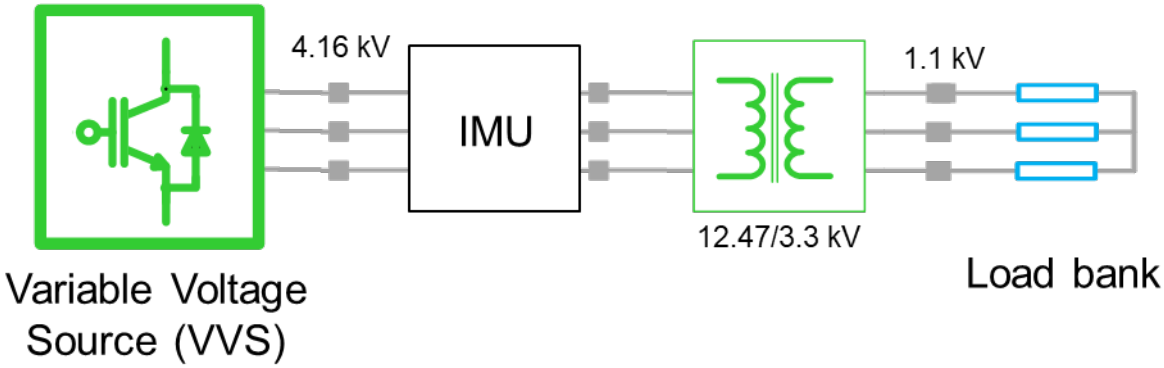


Figure 14. Test setup for medium-voltage AC impedance measurement

Issues experienced and mitigation measures

In some tests spurious trips of the controls were noticed. As a mitigating measure, the control boxes (see Figure 15) were moved from their initial position, which was close to the common mode choke, to the back of the PEBBs, and the control box rotated upwards by 90 degrees to minimize coupling of magnetic fields.

Figure 15. Placing controls to minimize EMI

As was detected while testing, common mode current were a major issue. To some extent, these issues were expected due to the effective high switching frequency. As the high frequency is a design choice to allow inject controlled currents and voltages in the kHz-range, means to minimize the undesired common mode current have to be taken. Improvements were made by further isolating the PEBB capacitors from the metal frame, and the initially 50-70 nF of coupling capacitance could be reduced to about 4-6 nF (see Figure 16).

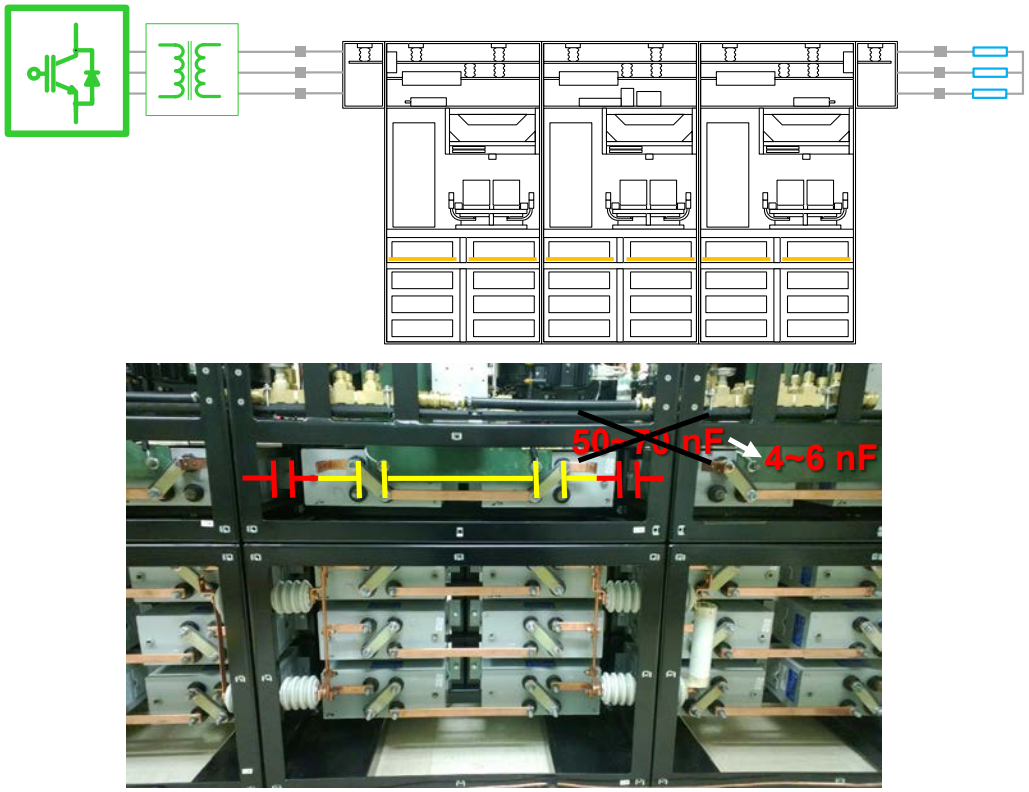


Figure 16. Isolating PEBB capacitors

Another part of this common mode effect is depicted in Figure 17. The induced common mode currents intermittently triggered the DC-bus discharge relays and halted operation.

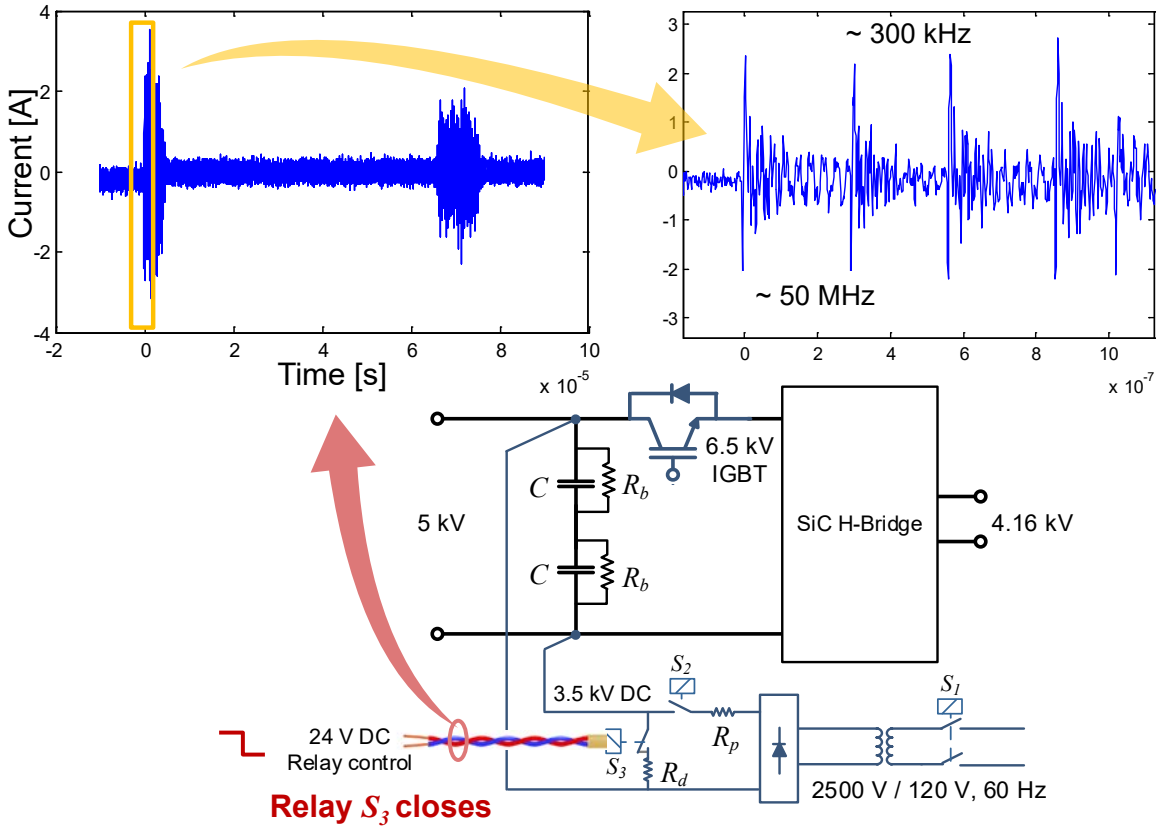


Figure 17. Common mode current triggering DC-bus discharge relay

Design improvements

Due to the issues experienced and reported above, the following two items were noted as possible improvements to future implementations.

1. **Improved module packaging**: the fast switching requires fast rising and falling gating signal, which in term seemed to have caused intermittent through-shooting event, i.e., caused both switches to turn on at the same time. Improvements will need to be made in the module design to avoid the cross-coupling in gating signals.
2. **Immunity to electromagnetic interference**: the higher switching frequency seems to have caused several issues, and more specifically, common mode issues. The parasitic capacitive coupling may play a much bigger role than initially anticipated, and component designs may have to be adjusted accordingly to ensure common mode currents are kept low.

7 Summary

This project was the first successful application on an impedance measurement unit at the medium voltage level. The IMU was developed by CPES, and tested using the medium voltage facilities at CAPS. Both AC- and DC-system setups with the Power Electronics Building Blocks and Impedance Measurement Unit operating in several configuration were used to evaluate capabilities. This report details preparation, setups, procedures, test results and analysis, and problems encountered and mitigation measures taken. The team was not successful in progressing to tests at the design voltage level of 4.16 kV, but several issues were overcome to allow demonstrate the IMU at 2.8 kV.

Two main possible root causes were identified for possible future improvements. It is anticipated that addressing the issues of **SiC-module design**—improving behavior at the higher switching frequencies, and **common mode sensitivity**—reducing parasitic coupling, will allow to fully bring the IMU-technology to the voltage and power levels required for anticipated advanced electric shipboard power system designs.

After the medium voltage and power stage testing ended at CAPS, the main controller and corresponding interfacing hardware remained at CAPS to allow set up a Controller Hardware-in-the-Loop platform. This setup can be used to determine the impedance characteristics of modeled subsystems as used, for example, in Power HIL simulation based testing (an overview is given in Appendix D).

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Appendix A. Test Facility Equipment

The following summarizes the test equipment used in the experiments.

Table 2. FSU-CAPS Test Equipment

Equipment	Description	Data
VVS	Variable Voltage Source	0-4.16 kV_{AC} (5 MW/2.5 MW) and/or 0-1.15 kV_{DC} (2.5 MW) variable voltage source
MMC	Modular Multi-Level Converter	Four 1.25 MW, 0-6 kV, 210 A converters, supplied at 3.3 kV, 60 Hz
Resistive load bank	Configurable resistive load bank	Twelve 3.4 ohm, 80 A resistors
3-phase resistive load bank	Switchable resistive 3-phase load (Avtron)	240 or 480V, power levels: [5 10 20 20] kW
RTS	Real time digital simulator, RTDS® from RTDS Technologies	The RTS controls and protects all experiments; provides references for the DUT, and triggers data captures. RTS time step is 50 us.
NI-DAQ	National Instruments data acquisition	NI-6133

Appendix B. IMU Data

The following table provides the salient specification data of the medium impedance measurement unit.

Table 3. IMU Specifications

IMU Configuration	Description	Data
3 PEBB units	Each PEBB is an H-bridge with filter inductor (AC-side) and capacitor (DC-side)	$L_{f1} = L_{f2} = 1$ mH, $R_{Lf} = 30$ mOhm, $C_{dc} =$ 0.5 mF + 1.5 mF per PEBB, $f_{sw} = 10$ kHz, $T_{DT} = 2$ us, effective $f_{sw} = 60$ kHz, each PEBB max. current: 50 Arms (note: de-rated from 100 Arms); Each leg based on 10 kV, 120 A SiC MOSFET modules with JBS diode. Cdc: eight 850uF x1/2 or x4/2
AC impedance measurements	range: 0.1 Hz – 1 kHz	System frequency: 60, 400 Hz, $S_{system,\ max} =$ 1.1 MVA, voltage: 4.16 kV, system current: 3x50 = 150 A
DC impedance measurements	range: 0.1 Hz – 1 kHz	System frequency: DC, voltage: 6 kV, $S_{system,\ max} = 0.9$ MW, system current: 3x50 = 150 A
Shunt configuration	Connected between two phases. Intended for source output impedance evaluation.	Up to 5% I_{nom} current injected
Series configuration	Connected as part of one phase, all three PEBBs in parallel with a capacitor. Intended for load input impedance evaluation.	Up to 5% $V_{nom,p\text{-}n}$ voltage injected

Appendix C. Double-pulse Test Equipment and Procedure

The following provides detailed information on equipment necessary and procedure used in the double-pulse tests.

Table 4. List of equipment (double-pulse test)

Equipment	Purpose(s)	Part #	Mfg.	Specs	Qty.
High-voltage passive probe	V_{DS} measurement	P6015A	Tektronix	20 kV DC, 75 MHz	1
Rogowski Coil	I_D measurement	CWT Ultra Mini	PEM	600 A	1
Low-voltage differential probe	V_{GS} measurement	TDP1000	Tektronix	42 V, 1 GHz	1
Inductor (1 of the 2 in the PEBB)	DPT inductor	-	-	L= 2mH/4, EPC= 290pF/2	1
Function generator	Produce double-pulse waveform	AFG3102	Tektronix	-	1
Low-voltage dc power supply	To supply +15 V to the gate drive	E3631A	Agilent	0 - ±25 V, triple output	1
High-voltage power supply with remote	For V_{DS} supply	203/303L	A.L.E. Systems	15 kV	1
DMM	Testing setup	-	-	-	1
Oscilloscope	Waveform capture	MSO5104	Tektronix	1 GHz, 10 GS/s, 4 Channels	1
Fiber optic transmitter	Transmits the signal from the function generator to the module and IGBT gate drives	T-1521	Avago	5 MBD	2
Optical fiber cable	To transmit the signal from the transmitter to the receiver on the module and IGBT gate drives	-	-	-	2
BNC split cable	Connect function generator output to module and IGBT transmitters	-	-	-	2
High-voltage differential probe	V_{GS} measurement of top switch	P5210	Tektronix	5.6 kV differential, 50 MHz	1

1. Testing setup (assuming the bottom switch is to be switched)

a. Adjust the high-voltage and low-voltage probes.

   ☐ If necessary, change the "offset" of the channel on the oscilloscope to zero the waveform. Make sure to adjust the MATLAB "get_waveforms.m" code to account for this offset.

b. Isolate the module not being tested from the dc bus.

c. Secure the Rogowski coil around the copper pillar that connects the source terminal of the bottom switch in the module to be tested to the negative of the dc bus.

d. Connect the low-voltage differential probe to the gate and source terminals of the bottom switch. For this connection, flying wires have been soldered to the gate drive board near to the connection to the module.
e. Set the oscilloscope to edge trigger on the first falling and second rising edges of the gate-source voltage waveform to capture the turn off and turn on switching events, respectively.
f. Connect the high-voltage passive probe to the drain and source terminals of the bottom switch.
g. Connect the gate drive to the module to be tested. Ensure that the proper gate resistors on the gate drive.
h. Set the voltage of the low-voltage dc power supply to 15 V. Connect the supply to the gate drivers on all four modules. Set the current limit accordingly.
i. Connect the function generator output to the module and IGBT gate drive fiber optic transmitters using BNC split cables.
j. Set the function generator amplitude to 3 V, the offset to 1.5 V, and the output impedance to 50 Ω (this gives 60 mA). The double-pulse signal can be sent using LabVIEW code. After setting the double-pulse signal, use the arbitrary waveform for the other channel of the function generator to send a constant ON signal (2.5 V amplitude is sufficient) for the IGBT.
k. Connect the gray side of the optical fiber cables to the transmitters, and the blue sides to the receivers on the module and IGBT gate drives (make sure the channel with the double-pulse signal goes to the module gate drive, and the channel with the constant ON signal goes to the IGBT gate drive).
l. Connect one of the PEBB inductors to the switching node (common node between the top and bottom switches) and the drain of the top switch (positive of the dc bus). The anti-parallel diode of the top switch will be used as the free-wheeling diode (FWD).
m. Connect the chiller to the high-voltage power supply (optional).
n. Connect the high-voltage power supply to the dc bus. Ensure that the remote and chiller are working properly prior to connection.

2. Double-pulse test procedure

Note: Each box (□) in the following procedure list must be checked with a check mark indicating that the step was performed. This must be done every time this testing is executed. The entire procedure should then be signed by all persons conducting the testing, and filed for future reference. This file, along with all test run records, must be available to Lab Management upon demand.

a. Before the experiment begins

- ☐ Visually verify that all power supplies are turned off.
- ☐ Ensure that the current limit on each supply is set accordingly.
- ☐ Manually check that all connections are secure and correct (use DMM to verify electrical connections).
- ☐ Ensure that all safety guards are in place.
- ☐ Turn on the chiller for the high-voltage power supply (optional).
- ☐ Turn on the +15V low-voltage dc power supply for gate drivers.
- ☐ Ensure that the current draw on the power supply is appropriate.
- ☐ Trigger a double-pulse from the function generator with no voltage on the dc bus.
- ☐ Ensure that the gate-source voltage waveform is correct on the oscilloscope.
- ☐ Check that the IGBT is ON.

b. During the experiment

- ☐ Use the remote to slowly increase the dc bus voltage from the high-voltage power supply.
- ☐ Trigger the function generator at a safe distance, starting with a low voltage and current level.
- ☐ Monitor and/or capture the oscilloscope waveforms.
- ☐ Slowly increase the voltage and current, stopping at reasonable intervals to trigger the function generator and capture the waveforms.

c. Shutdown procedure

- ☐ Gradually reduce the high-voltage power supply voltage to zero using the remote.
- ☐ Turn off the high-voltage power supply using the remote.
- ☐ Wait the necessary time for the capacitors to discharge through the bleeding resistors.
- ☐ Check that all meters read low or no voltage.
- ☐ Turn off the +15 V low-voltage dc power supply for the gate drivers.

Appendix D. Controller Hardware-in-the-Loop (CHIL)

After the PEBB/IMU testing in the medium voltage laboratory, a Controller HIL will remain at CAPS to allow collecting impedance data for salient equipment as modeled in simulation setups. Figure 18 depicts the CHIL concept. The controller is provided with measurements from the real-time simulated system, and the controller's firing pulses are fed back into the simulation after converting to the equivalent modulation index.

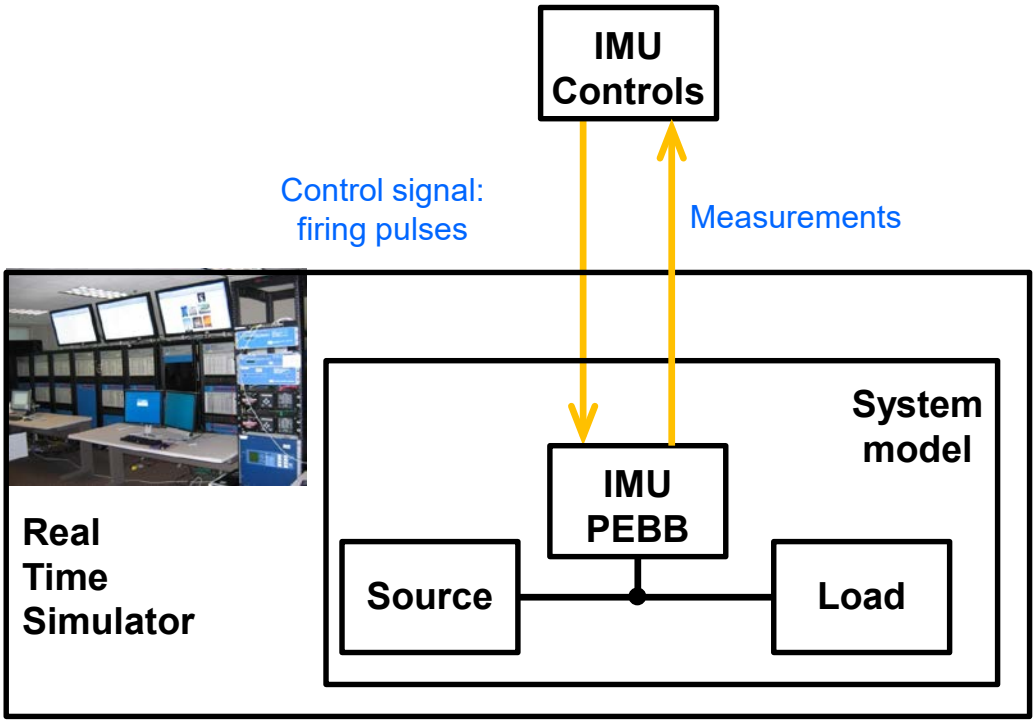

Figure 18. IMU CHIL overview