TASK 4.2.1
FAULT MANAGEMENT IN FAULT CURRENT LIMITED MVDC SYSTEMS

Year One – Deliverable(s)

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1 TASK DESCRIPTION

The characteristic of the rotating machines, which normally dominate the system behavior under fault conditions in AC systems, can be completely decoupled from the MVDC distribution system if certain converter topologies such as full bridge modular multi cell (MMC) converters or “active power distribution nodes” are employed. Note, that while SCR-type converters can interrupt fault currents at the next zero crossing of the AC current significant transients remain on the DC side. Moreover, fast interruption may not leave enough time to identify the fault location in meshed systems. However, employing converters which limit the fault current on the DC side to levels around nominal current values open up the opportunity to essentially eliminate the impact of high transient fault currents on the MVDC side. This in turn is expected to have substantial impact on the overall MVDC system design (no DC breakers, substantially reduced bracing against dynamic forces, etc.). Therefore, building upon work conducted previously at USC, this subtask seeks to develop and demonstrate a complete "fault current free" MVDC system.

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2 YEAR ONE DELIVERABLES

- Report “breaker free” MVDC system feasibility substantiated by initial experiments at the MW scale, including size and weight information for assessment in S3D.

3 APPENDIX OF REPORTS SUBMITTED

A. FY 14 Deliverables Report – Fault Management in Fault Current Limited MVDC Systems

APPENDIX A

FAULT MANAGEMENT IN FAULT CURRENT LIMITED MVDC SYSTEMS

FY 14 Deliverables Report

Task 4.2.1

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Abbreviations used

ABB	ASEA Brown Boveri
AMU	Analog Merging Unit
CAPS	Center for Advanced Power Systems
CFM	Centralized Fault Management
CHIL	Control Hardware In Loop
CPL	Constant power load
CPU	Central Processing Unit
DAB	Dual Active Bridge
DSP	Digital Signal Processor
EDS	Electrical Distribution System
ESRDC	Electric Ship Research and Development Consortium
FPGA	Field Programmable Gate Array
FSU	Florida State University
HIL	Hardware In Loop
HVDC	High Voltage DC
LFM	Local Fault Management
MMC	Modular Multi Cell
MVDC	Medium Voltage DC
p.u.	Per Unit
PED	Power Electronic Device
PHIL	Power Hardware In Loop
PI	Proportional Integral
PLECS	Piecewise Linear Electrical Circuit Simulation
PWM	Pulse Width Modulation
ROS	Rest of System
RT	Real Time
RTDS	Real Time Digital Simulator
SCR	Silicon Controlled Rectifier
STATCOM	Static Synchronous Compensator
UPS	Uninterruptible Power Supply
USC	University of South Carolina
VSC	Voltage Source Converter
VVS	Variable Voltage Source

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1 EXECUTIVE SUMMARY

In order to meet the constantly increasing power demand on notional US navy combat vessels, the Electric Ship Research and Development Consortium (ESRDC) is exploring different baseline models for shipboard power distribution system design including at medium voltage direct current (MVDC) levels. Although MVDC distribution systems are expected to provide advantages in terms of efficiency, reliability, and flexibility, concern remains over the means to de-risk such systems against short-circuit faults, ground faults, and open-circuit ("series") faults. In fact, traditional fault protection schemes based on circuit breakers are generally not readily applicable for MVDC distribution systems. Therefore, this task focuses on assessing and development of a novel fault management approach that provides protection, reconfiguration, and rapid restoration against short-circuit faults in MVDC shipboard systems.

The characteristic of the rotating machines, which normally dominate the system behavior under fault conditions in AC systems, can be completely decoupled from the MVDC distribution system if certain converter topologies, such as full bridge modular multi cell (MMC) converters [1] or active power distribution nodes [2], are employed. While SCR-type (i.e. thyristor based) converters can interrupt fault currents at the next zero crossing of the AC current significant transients remain on the DC side. Moreover, fast interruption may not leave enough time to identify the fault location in meshed systems. However, employing converters which limit, yet sustain the fault current in a controlled manner on the DC side to levels around nominal current values, open up the opportunity to essentially eliminate the impact of high transient fault currents on the MVDC side completely. This in turn is expected to have substantial impact on the overall MVDC system design (no DC breakers, substantially reduced bracing against dynamic forces, etc.). Therefore, building upon work conducted previously at USC [3-6], this task seeks to develop and demonstrate a complete "high fault current free" (i.e. fault current limited) MVDC system within 3 years (FY14 – FY16). This report provides details on the work conducted in FY14. This is not a final technical report on the subject of fault current limited MVDC systems. A detailed report on prior work on fault current limiting methods is contained in [7].

This report explains the various approaches and methodologies considered to achieve the overall aim of the research. The key subtasks which contribute to the combined efforts of FSU and USC are:

1. Modular multi cell (MMC) converter studies
2. Coordination of DC-DC converters
3. Centralized fault management (CFM)
4. Local fault management (LFM) mainly as a back-up to support CFM

Each subtask mentioned above contains corresponding analyses and simulation results details of which throughout this report.

MMC converters are an essential enabling technology to achieve fault current limiting particularly in an MVDC system. An important challenge which involves fast current limiting is coordination of controls of power converters. This in turn includes the coordination of both, the MMC converters used as source-side rectifiers as well as DC-DC converters at the zones or load-side. Understanding this issue of coordinated controls requires research into converter topologies, control schemes in addition to fault detection and identification. Fault detection and identification approaches are dealt with under the CFM related research. An alternative approach also lending redundancy is the LFM network. Another vital part of this work is the integration of CFM and LFM with the MVDC testbed at CAPS-FSU for experimentation to verify and validate results, which is an important part of planned work.

This report is divided as follows:

1. Section 2: Introduction to general research field with overview of specific research conducted.
2. Section 3: MMC converter control studies for integration into the notional MVDC power system with simulation results.
3. Section 4: Detailed explanation on issues related to coordination of downstream DC-DC converters and analyses to compute related parameters.
4. Section 5: CFM methodology and its applications to the MVDC system.
5. Section 6: LFM methodology and its differences with the CFM approach.
6. Section 7: Further planned research in addition to experiments to be conducted using the MVDC testbed at CAPS.

This report is supplemented with Appendix-A which shows standard p.u. normalization calculations applicable for the MMC converter studies and Appendix-B which shows MATLAB code used to run testbed experiments

2 INTRODUCTION

This section briefly mentions related research in the arena of system level fault management. The main body of this section explains the specific work carried out at CAPS to address issues related to task 4.2.1 including approaches used and future directions.

2.1 Related research – System level fault management

This subsection touches upon the various research into fault current limiting techniques carried out within this task. The aim is to underpin the differences between these approaches and the current work undertaken under this task. Figure 1 shows the representative system used for the bulk of this research subtask. Abbreviations and nomenclature used in Figure 1 are explained as follows:

1. **Power sources:**
    a. Main generator 1 (Main G1)
    b. Main generator 2 (Main G2)
    c. Auxiliary generator 1 (Aux G1)
    d. Auxiliary generator 2 (Aux G2)
2. **Power converters:**
    a. AC-DC rectifiers: Abbreviated “RECT” with number
    b. DC-DC converters: Abbreviated “CONV” with number
    c. DC-AC inverters: Abbreviated “INV” with number
3. **Propulsion:**
    a. Port side motor (Pmotor) where P stands for port
    b. Starboard side motor (Smotor) where S stands for starboard
4. **Power distribution:**
    a. Cable section abbreviated as CS with number
5. **General names:** Radar, zone with number and various nodes in the system are also numbered.

Table 1 shows the respective values of devices considered. The base voltage is 6 kV which is within the prescribed MVDC range as mentioned in IEEE Std. 1709 of 1kV to 35kV.

Device abbreviation	Rated power (kW)	Voltage (V)
Main G1	36,000	6000
Aux G1	4,000	6000
Main G2	36,000	6000
Aux G2	4,000	6000
Pmotor	36,500	6000
Smotor	36,500	6000
RECT1	36,000	6000
RECT 2	4,000	6000
RECT 3	4,000	6000
RECT 4	36,000	6000
INV1	36,500	6000
INV2	36,500	6000
CONV1	3,000	6000
CONV2	3,500	6000
CONV3	4,000	6000
CONV4	3,000	6000

Table 1 Power ratings for devices used for analysis

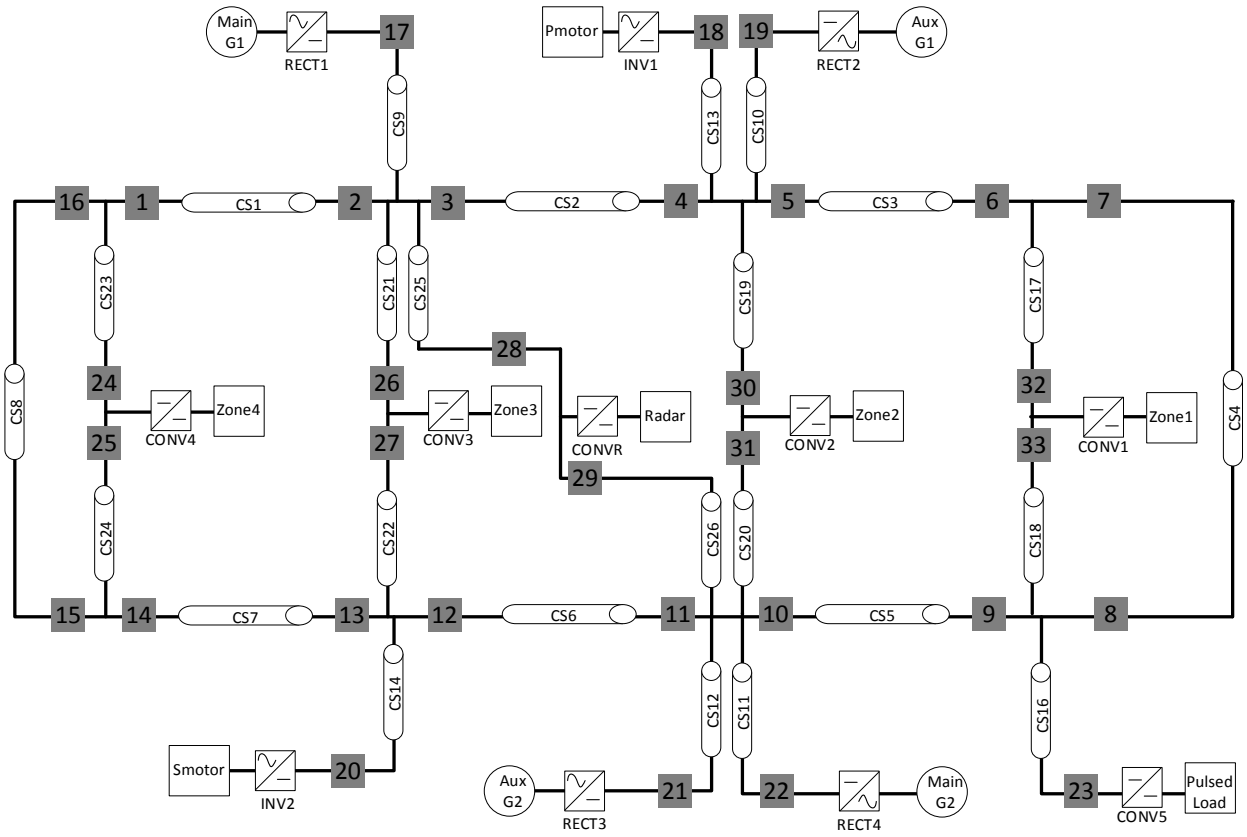


Figure 1 Notional Ship MVDC Power System Topology

There exists no natural zero crossing point for current in DC systems and currents must be forced to zero using some external means [4]. Alternating currents naturally cross zero every half-cycle giving an

opportunity for mechanical circuit breakers to break the. Commonly used conventional AC circuit breaker are not readily applicable for DC applications in general [4]. Thus, a significant challenge in the MVDC shipboard system is the fault protection.

The issue of MVDC protection has led to efforts to develop solid-state or hybrid circuit breakers for MVDC systems [8]. On the other hand, a multi-functional power converter that can actively control the power may limit the fault current in short time [10]. A breaker-less fault protection scheme in MVDC system is stated in [11]. It is based on the inherent protection capability of power converters and the power system architecture. Figure 2 illustrates the MVDC power system architecture proposed in [10].

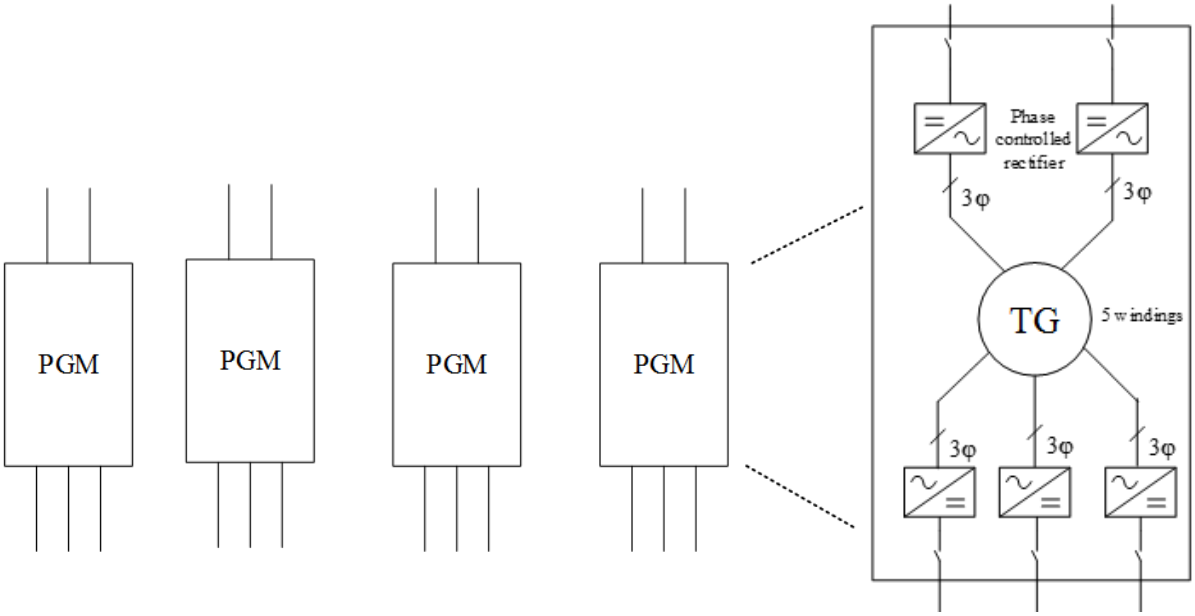


Figure 2 Breakerless MVDC architecture [9]

The power sources of the system are four Power System Modules (PGM). Each PGM consists of one 30 MW Multiphase Turbine-Generator (TG), each with five sets of windings and each set of windings feeds one individual SCR based six-pulse phase controlled rectifier. Totally, there are twenty individually controlled power sources in the system. At the occurrence of a fault, only those power sources in which fault occurs will be cut off from the system and the remaining healthy power sources continue operation. Therefore, minimum power reduction and high stability and survivability can be potentially achieved. Cutting off a power source is achieved by shutting down the rectifier instead of opening circuit breaker. Utilization of the power electronics devices enables faster fault protection compared with using mechanical circuit breakers.

However, SCR fundamentally is a semi-controllable device. As a result it will not turn off instantly after suspending the gating pulses until the conducting current reaches zero and the zero-current crossing point occurs every half-cycle. Thus, the shut-down of the SCR based rectifier is slower than using controllable devices such as IGBT. Hence, the protection time can potentially be made even shorter. In general, limitations with this proposed scheme are as follows:

- Long recovery time as it is needed to restart the converter and charge DC link capacitor
- High fault current stress due to semi-controllable SCRs
- Un-centralized structure owing to the Lack of a DC bus, central control and connection between parts

While in principle the necessary fault location and isolation can be implemented via localized control and traditional differential protection relaying schemes this task will explore the advantages expected from the CFM approach. In particular, the digitally net-worked utilization of multiple sensor information already available in a power electronic based MVDC system is expected to substantially enhance robustness and adaptability of the proposed fault management approach. The fundamental advantages of the CFM approach can be briefly stated as:

a. Its ability to include a wide range of sensor information for locating faults in fault current limited systems
b. Simplified protection coordination
c. The stronger integration of system protection with converter control.

The key enabling technology for such a system is the advancement of digital communication capabilities which can meet the stringent real-time requirements posed by such a system. This task will develop a framework for designing CFM overlays for MVDC systems. The task will test this concept via the FSU's cyber-physical RT system simulation test bed. Therefore, this task will adapt the FSU's cyber-physical RT simulation test bed with the corresponding real-time sensor communication hardware to facilitate meaningful testing of the approach in real time.

2.2 Research work at FSU and USC under task 4.2.1

This work is conducted in close collaboration with Dr. Herb Ginn and the team at USC. Their contributions are in the field of multiple-module-converter (MMC) control and small-scale hardware experiments and also to refine and adapt a previously developed fault detection approach which is different than the one pursued by FSU. The USC approach lends itself well as a backup for the primary protection provided by FSU's Centralized Fault Management (CFM) approach. USC's test environment was insufficient to scale up the fault interruption approach to medium voltage. The joint-research conducted will help compare the two fault detection approaches and allow USC to validate their experimental results on fault interruption at higher voltage and power levels at the FSU lab. Regular discussions and meetings between collaborators have resulted in a substantial body of research work pertaining to this task. The overall work could be categorized into various individual topics as elaborated in this subsection.

2.2.1 Protection challenges of the MVDC system

The MVDC system is formed as a looped structure with multiple energy sources and associated power electronic devices (PED) for better efficiency and reliability. However, the change of structures and the integration of PED devices introduces challenges to the design of the protection systems which are listed below.

1. The primary challenge arises from the change of structures. The looped structure will have significantly different dynamic behavior during fault conditions as compared to the traditional distribution systems, which are normally in radial structures and supplied by a single source.
2. The second challenge is the highly distorted fault current waveform and bi-directional power flow from the PEDs and the local generators.
3. The third challenge is the requirement of adaptability. The protection systems must be able to accommodate the dynamic operating conditions of the MVDC system with multiple controllable PEDs.
4. The last challenge is the extreme fast protection requirement of the MVDC system (Figure 3). Section 2.2.2 provides a detailed explanation for an initial guideline of an 8 ms system restoration time that is expected to reduce the fault impact of the generators and of the load to a minimum.

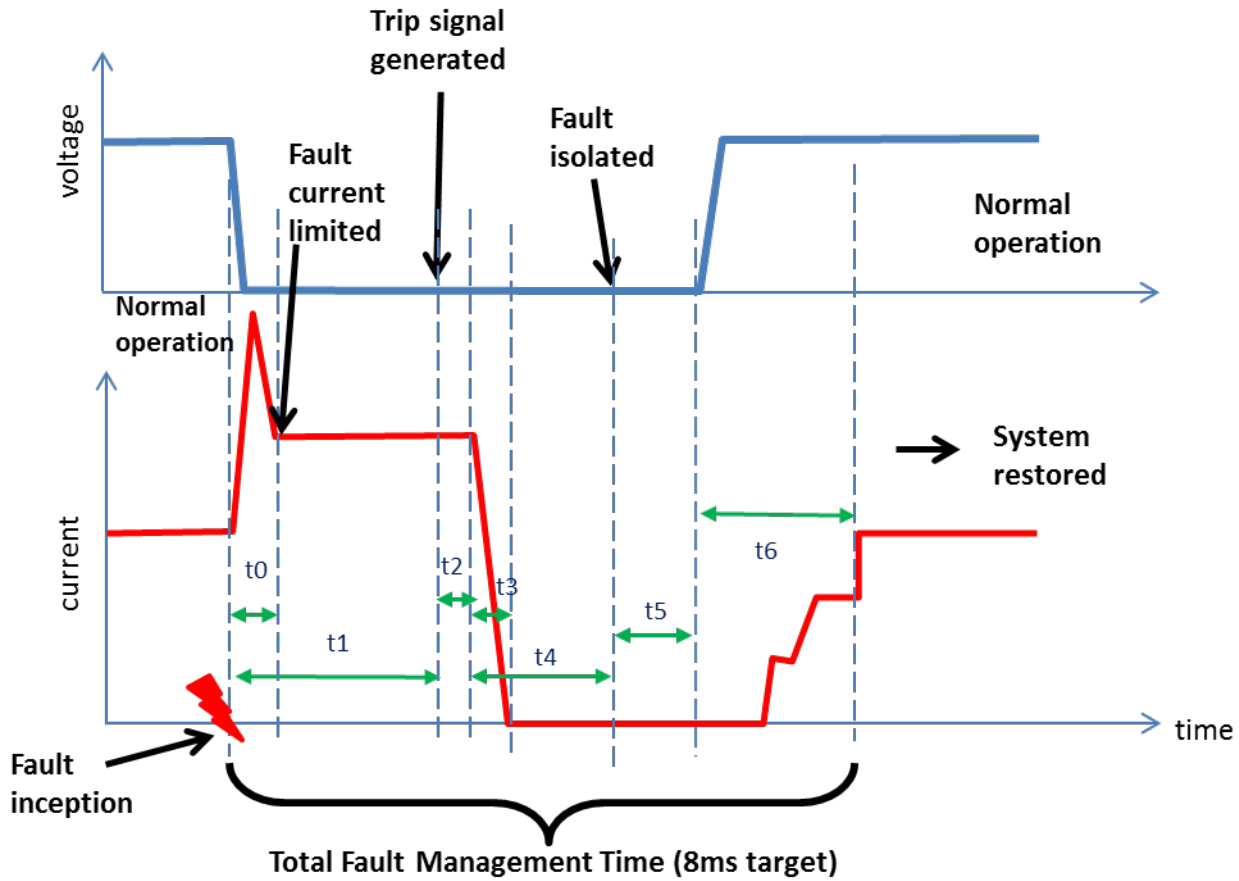
2.2.2 Overall aim and preliminary target

Since the MMC converters are an essential enabler for the “high fault current free” MVDC system, this task also focuses on the development and demonstration advanced control strategies for those converters. The challenge emerges from the need to implement a fast DC side control to facilitate ultra-fast fault current limitation under all system conditions. Moreover, the control needs to coordinate several MMC and other converters working simultaneously during severe disturbances. The objective is to develop and demonstrate such control strategies via non-real-time simulations, then real-time simulation, and eventually verify them via experiments at power levels up to 1 MW.

Another objective of this task is to develop design and control guidelines for isolated DC-DC converters which serve as the zonal power feeds in MVDC shipboard power systems. Those converters have to operate in close coordination with the MMC converters to facilitate the overall response expected from the proposed system approach. In particular, they need to (a) not contribute additional fault current, (b) provide UPS functionality for the zonal loads during the short power interruption on the MVDC side, and rapidity resume their normal operation after the fault has been cleared. This requires special considerations for their hardware and control design. This task will develop and test feasible approaches to achieve those goals via non-real-time and real-time simulation.

Ultimately, this task aims at demonstrating the “high fault current free” MVDC system by utilizing CAPS-FSU’s new MVDC lab with up to 4 MMC converters at MV levels (ca. 5 kV) and meaningful power levels (ca. 1 MW). This task will execute experiments to demonstrate that faults can be regulated and cleared by MMC converters. Rapid reconfiguration immediately after a fault has been cleared will also be demonstrated. Moreover, experiments will be conducted to investigate basic MVDC arc fault behaviors under severely fault current limited conditions. Eventually, the CFM scheme will be integrated with experiments in the MVDC lab to demonstrate that a fault locations can be identified and cleared fast enough and power can be resorted via no-load disconnect switches in time frames substantially shorter than those currently governing AC protection concepts.

The target is to complete the entire sequence between fault occurrence and full system restoration in 8 ms. The rationale for this timing target that it is equivalent to ½ cycle of a 60 Hz system and hence is expected to lead to an almost benign event if achievable. Moreover, it is very ambitious and expected to push the envelope of feasibility. However, the optimal time for completing the sequence will eventually be determined by many factors at the system level. It may well turn out that the cost for achieving the 8 ms target is too high. Nevertheless, this research task aims to provide insight into the corresponding trade-off space to better understand cost driving factors. Figure 3 offers a view of the various amounts of time expected to be needed for the proposed CFM operations.



Where:
t0 = Current limiting response delay, t1 = CFM/LFM response delay, t2 = Trip signal delay, t3 = Convertors shut down delay, t4 = Disconnected opening delay, t5 = Idle time, t6 = Power restoration time

Total fault management time= t1+t2+t4+t5+t6

Figure 3 Comparative view of time scales considered for protection

2.2.3 MMC converter control

A MMC converter control derived from the conventional voltage source converter control will be implemented in MATLAB/Simulink for the systematic design and control strategy verification. It is important to note that commercially available controller ABB-AC800PEC and the already developed USC universal controller platform will form the major part of the overall control scheme. However, since in this specific case, coordination between the MMC converters and zonal converters is essential, for certain aspects of the controller design process, attention will be paid on the fast DC side control and energy balance within MMC converter. The former is the requirement of fault current limit capability, and the latter is the special requirement for the MMC converter control. It is necessary to note that an entirely novel control scheme is not a driving requirement for this research. The MMC converter control will be verified by using two different real-time simulators with the corresponding controller hardware in loop (CHIL) setups.

1. **CHIL-1** – This is the recently commissioned setup of two MMC controllers mirroring the actual controllers used in the FSU MVDC lab. The controller hardware and software is the commercial

product AC800PEC provided by ABB as part of the FSU MVDC lab installation. The real time simulator in this case is RTDS. The interfacing of the 288 firing pulses and associated analog measurements of voltages and currents use the traditional analog wiring approach as it interfaces at the local cell controller level where it otherwise connects with firing pulses to the IGBT drivers in the real converter. This setup is primarily used to de-risk high power experiments in the FSU MVDC lab. Moreover, FSU has full access to the ABB proprietary control software under an existing non-disclosure agreement. Therefore, FSU researchers will be able to alter portions of the control according to the needs of the project.

2. **CHIL-2** – This is a separate setup which will utilize the universal controller hardware developed by USC and OPAL-RT as the real-time simulation platform. The reasons for this alternate CHIL approach are: first, the corresponding controller hard and software, as developed by USC, is completely unrestricted and fully transparent to the researchers. Secondly, the setup will represent the corresponding low power hardware at USC and as such will serve as an excellent means to corroborate experimental results from USC. Third, both the USC controller and the OPAL-RT system offer the opportunity to interface the firing pulses and other control and feedback signals solely via fiber optic. This reduces the analog wiring substantially, if not entirely. Finally, while RTDS certainly could also facilitate a fiber optic based firing pulse interface, it is advantageous to employ a different real-time simulation platform in order to allow cross platform validation of the underlying rest-of-system models.

Both CHIL setups will eventually allow studies within multiple MMC converters for a full system study of the fault management approach.

2.2.4 Centralized Fault Management (CFM)

In order to achieve a reliable, robust, and yet ultra-fast mechanism to locate a (rail-rail) fault in a ring bus type system (as shown in Figure 1) we proposed to develop a (more) centralized fault management (CFM) approach. It takes the traditional protective differential relaying scheme to the next level. Multiple (current and voltage) sensor information is merged into the CFM units for decision making. The major research challenge in this activity is with the development of high-speed, hard real-time capable digital communication mechanisms which meet the timing and bandwidth requirements of the main task. In particular, different data routing topologies and protocols need to be investigated, modeled, and compared for a down select. The objective of this task is to develop adequate models to be used for system level design studies of CFM concepts.

The experimental setup envisioned for the final system level demonstration is shown in Figure 4. D1 and D2 are ultra-fast disconnect switches that could be used for fault isolation and bow-cross hull disconnection respectively. A more detailed diagram of the test setup in section 7.4.1 (Figure 38) is derived from Figure 4 and is explained in the respective portion of this report.

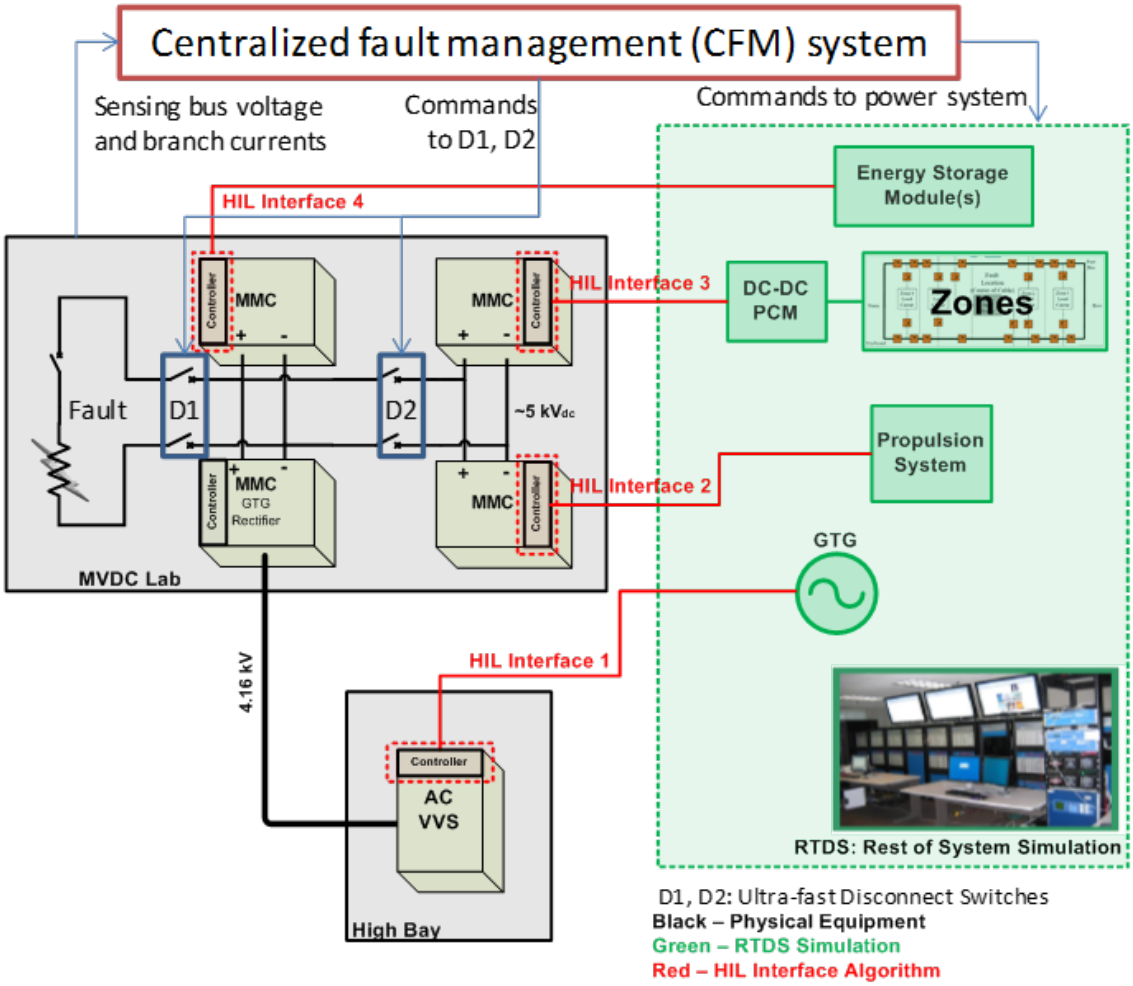


Figure 4 Overall system demonstration envisioned at FSU-CAPS

2.2.5 Control of DC-DC converters for fault ride through

The dual challenge for zone converter design lies in the paradox of meeting the requirement of input and output at the same time: to limit the current injection into DC bus during the fault period, the zone converter should have a small input capacitor; to maintain operation, the zone converter should have a capacitor large enough, otherwise the input voltage will fall dramatically and trigger the under-voltage or over-current projection of zone converter. This is in order to prevent the load side voltage to dip during the short MVDC-side voltage collapse at the occurrence of a fault.

This challenge is addressed in [11], by adding a high power diode between the large load-side capacitor and system DC bus. At the occurrence of a fault, the load-side capacitor was disconnected from the DC bus by the diode, while remained in connection with the load. Though this challenge has been solved, the method in [11] still has its disadvantages, including:

1. Additional diode loss
2. Large size capacitor
3. Need for current-limiting start up
4. Additional single-point-of-failure

The proposed approach in this research task seeks to address the above mentioned challenges with a DC-DC converter based solution. By choosing a proper topology and applying the best suited control strategy

proposed, the DC-DC converter will be able to operate under a wide input voltage range, especially during MVDC bus voltage recovery time. This feature enables the use of a small value for the converter input side capacitor without needing disconnection from the MVDC bus.

Setting up a set of common benchmarks relating to the parameter space and simulation models is important to ensure efficiency among the various participating contributors of this research task. A part of such benchmarks is available in ESRDC documentation including the baseline MVDC system model. Simulation models that may need to be developed specifically for this research are in three commonly used environments namely MATLAB/SIMULINK (or PLECS), RTDS and OPAL-RT.

Section-3 elaborates on the subtask involving MMC modelling. The control aspects and related studies are detailed and simulation results are explained. Section-4 discusses the work done relating to the control studies of DC-DC converters for fault ride through capability. Aspects of the dual active bridge topology are explained along with necessary parameter calculations. Section-5 details the developmental work towards the local fault management (LFM) approach at USC while section-6 contains information on the centralized fault management (CFM) approach developed at FSU. Section-7 discusses the current status of research work done in this particular task along with certain recommendations and plans for the near future continuation and progress.

3 MODELLING AND ANALYSIS OF MMC CONVERTERS

As elaborated in section 1, 2.2.3 and 2.2.5, MMC converters are a critical aspect of the overall research goal of fast fault current limiting within the shipboard MVDC power distribution system. This research does not relate to the design of MMC converters, but to their application within the specific constraints of an MVDC shipboard system with the set aims of:

- 8 ms : time for entire sequence of fault occurrence, detection, isolation and system restoration
- Coordination with other DC-DC converters

Thus, this section of the report is dedicated to MMC converter analysis and modeling/simulation studies carried out at CAPS-FSU with contributions from USC. The modeling and simulation of MMC is the preliminary study of the know-how of integrating MMC converter into MVDC system. The requirement of the quick system restart (described in Figure 3) is also taken into consideration. The MMC converter related parameters in this study are taken from the small scale platform at USC.

The simulation result will lead to a systematic design of MMC converter and control specifically for the MVDC power distribution network. The MMC converter application is well understood in the High Voltage DC (HVDC) scenario. However, using MMC converters in MVDC system is a relatively new domain for electric ship designers. Hence, a preliminary MMC converter analysis is imperative. The different design constrains between the HVDC and MVDC need to be evaluated during the simulation study.

The MMC converter modeling and design on the system level needs to build up a test benchmark system so that the performance of control and protection can be verified and compared. MATLAB/Simulink is a powerful tool for off-line modeling of the power electronics system. Before controller is implemented in hardware, the control strategy has to be verified in Simulink model. Hence, a MMC test system is implemented in Simulink and the following issues are covered:

- Modeling of MMC test system in Simulink
- MMC converter modeling
- P.U. normalization
- A conventional MMC controller implementation in Simulink
- Simulation results for start-up sequence and power delivery to a DC load

The following subsections elaborate MMC converter related studies, parameters of which are taken from the USC's small scale system (not MVDC scale) as a reference. Analysis and preliminary simulation results pertaining to the MVDC fault current limiting goal have also been outlined. Appendix-A provides detailed calculations on p.u. normalization used for the MMC converter system.

3.1 MMC converter, source and control

The MMC converter is a three-phase AC-DC system with six H-bridge cells in each branch and six branches. The inductor is inserted into each branch to limit the current. The converter is connected to the grid and a pre-charge circuit is used for charging the capacitor to an initial voltage. Figure 5 shows the architecture of the MMC test system that is modeled in Simulink. The MMC converter provides DC power supply to the load and connects the AC source through pre-charging circuit. The system overview in Simulink is given in Figure 6.

3.1.1 The cells

The cells are of full bridge configuration with an inductor in each branch. The phase-A implementation of the converter in Simulink is shown in Figure 7. A detailed view of the branch configuration is shown in Figure 8 (a) and (b). This simulation treats the grid as an ideal infinite source, however, to study the AC voltage support features need to weaken the source. The operational parameters are given in Table 2.

Parameter	Value
Number of cells per branch	6
Cell configuration	Full bridge (four IGBTs)
DC voltage of cells	133.33 V
IGBT internal resistance	1e-3 Ohms
IGBT Snubber resistance	1e5 Ohms
IGBT Snubber capacitance	inf
Capacitance of cell capacitor	0.015 F

Table 2 Operational parameters

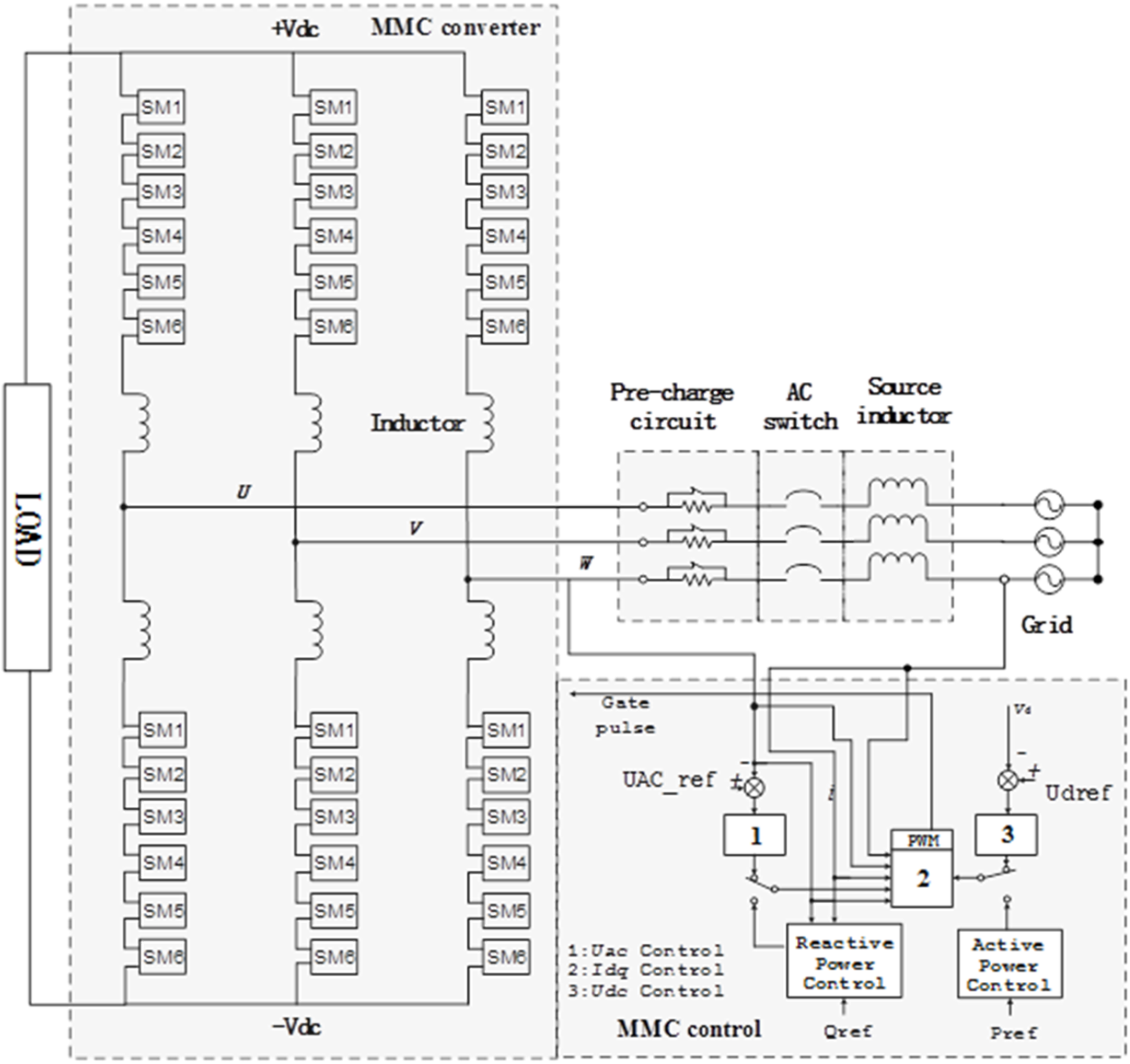


Figure 5 MMC test system in Simulink

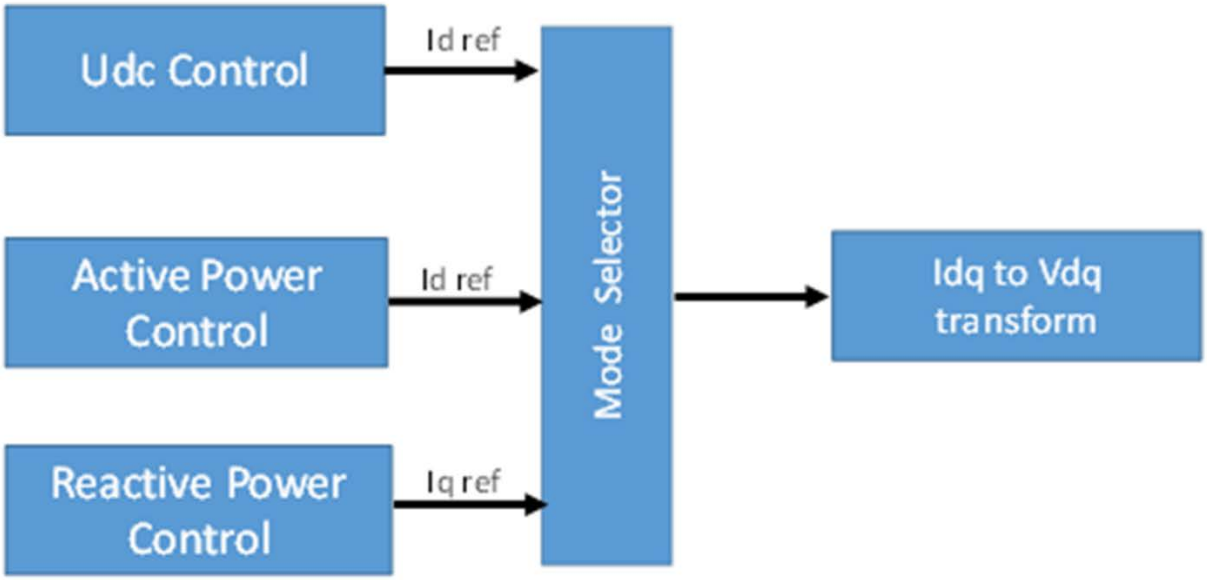


Figure 6 MMC core controls modelled in Simulink

3.1.2 The converter

At the converter level, the MMC is an AC-DC converter. The rated DC voltage is 800 V with nominal DC current of 100 A. On the AC side, the branch inductor of 1mH is inserted. The MMC converter consists of six branches with six cells in each branch in Figure 8(a). The branch model also shows the branch inductor and cells in Figure 8(b).

3.1.3 The source

The ideal AC source is connected to the converter to perform power exchange functionality between them. The parameters of the AC source are given in Table 3.

Parameter	Value
Phase to phase RMS	208 V
Frequency	60 Hz

Table 3 Parameters for AC source

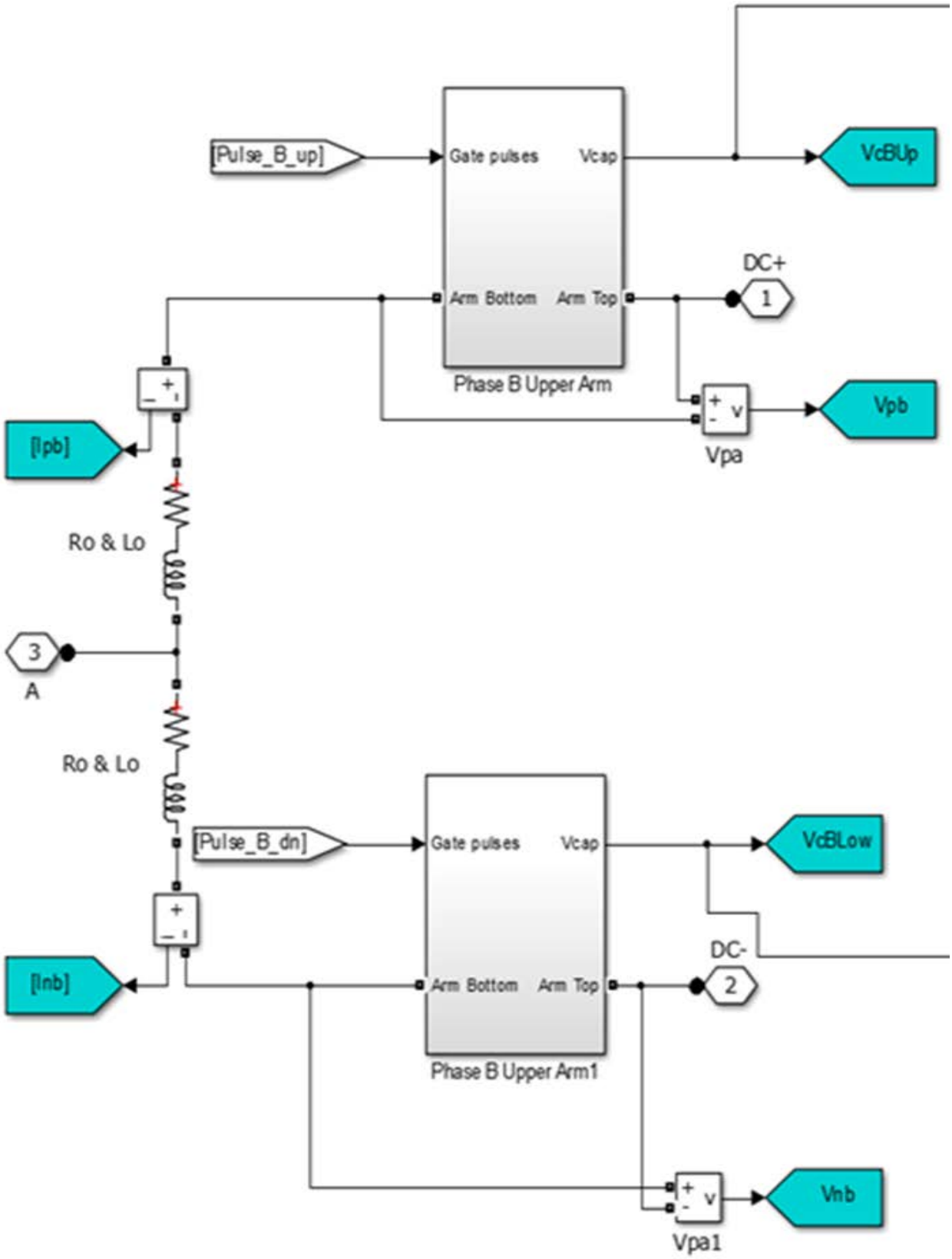
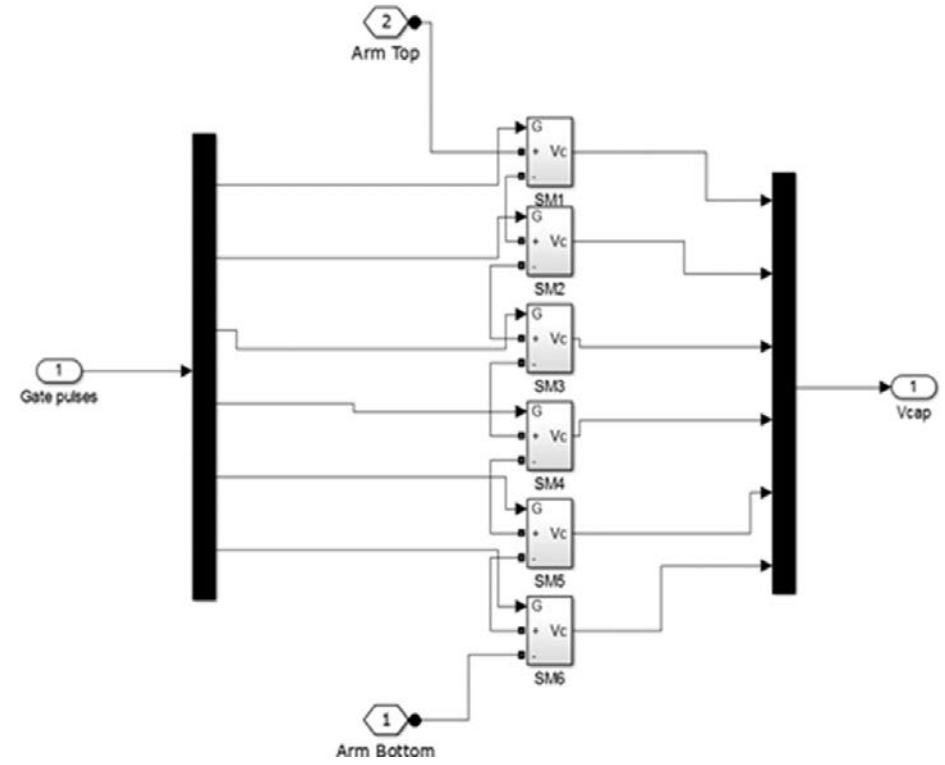
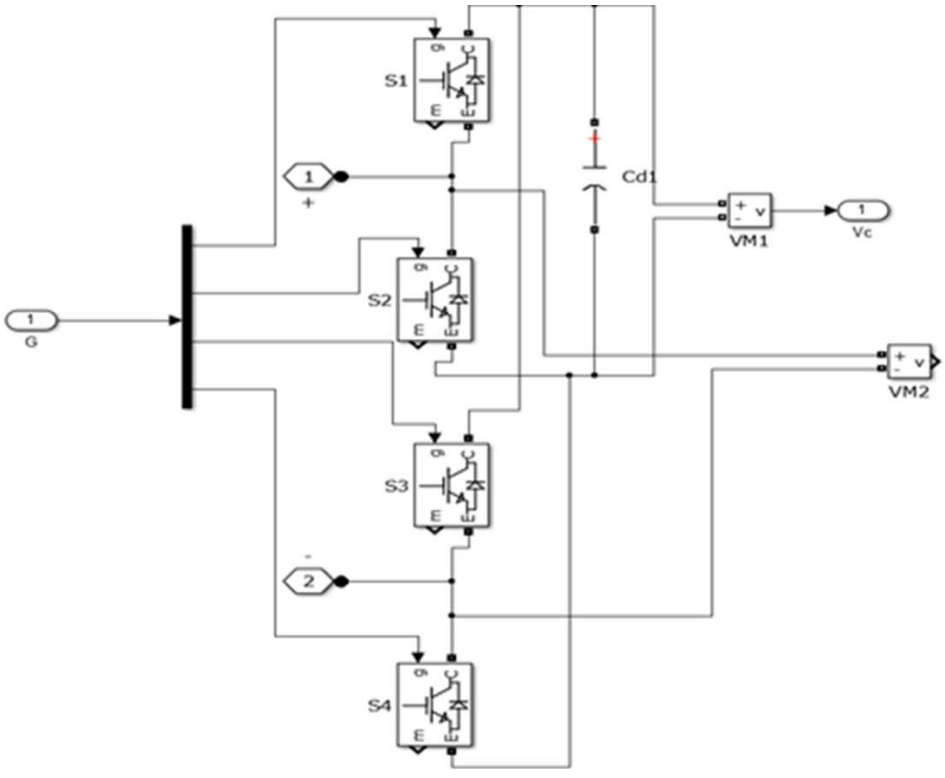


Figure 7 MMC converter phase-A



(a)



(b)

Figure 8 (a) Six cells in each branch (b) Inductors within each branch

3.1.4 MMC control

The controller depicted in [12], originally designed for reactive power compensation (Figure 9) is relatively straightforward. The STATCOM [12] does not need to transmit active power although the active power reference is still needed to compensate the loss in each power cell. The following controller is implemented in Simulink.

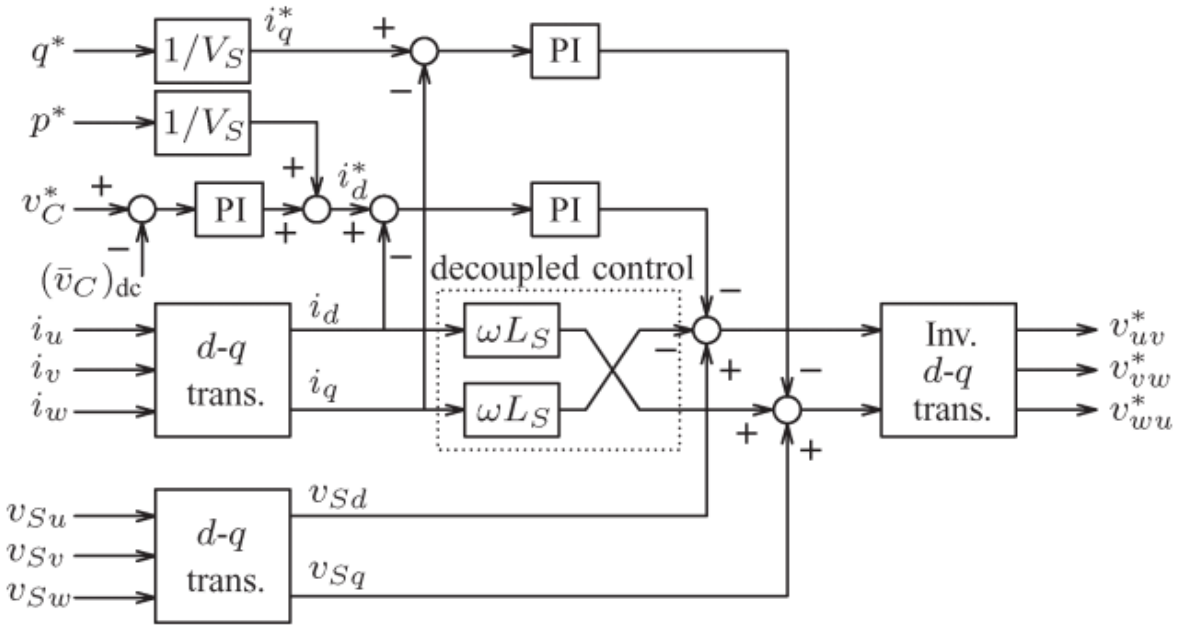


Figure 9 A STATCOM Control Diagram [12]

The conventional MMC control contains two control loops: the outer loop reference can be DC voltage, active power or reactive power, the inner loop is *d-q* current control loop. Figure 10 shows the MMC controller block, the *P*, *Q*, U_{dc} references are provided as configurable input. The output of the control blocks is the voltage reference which will be assigned to each branch.

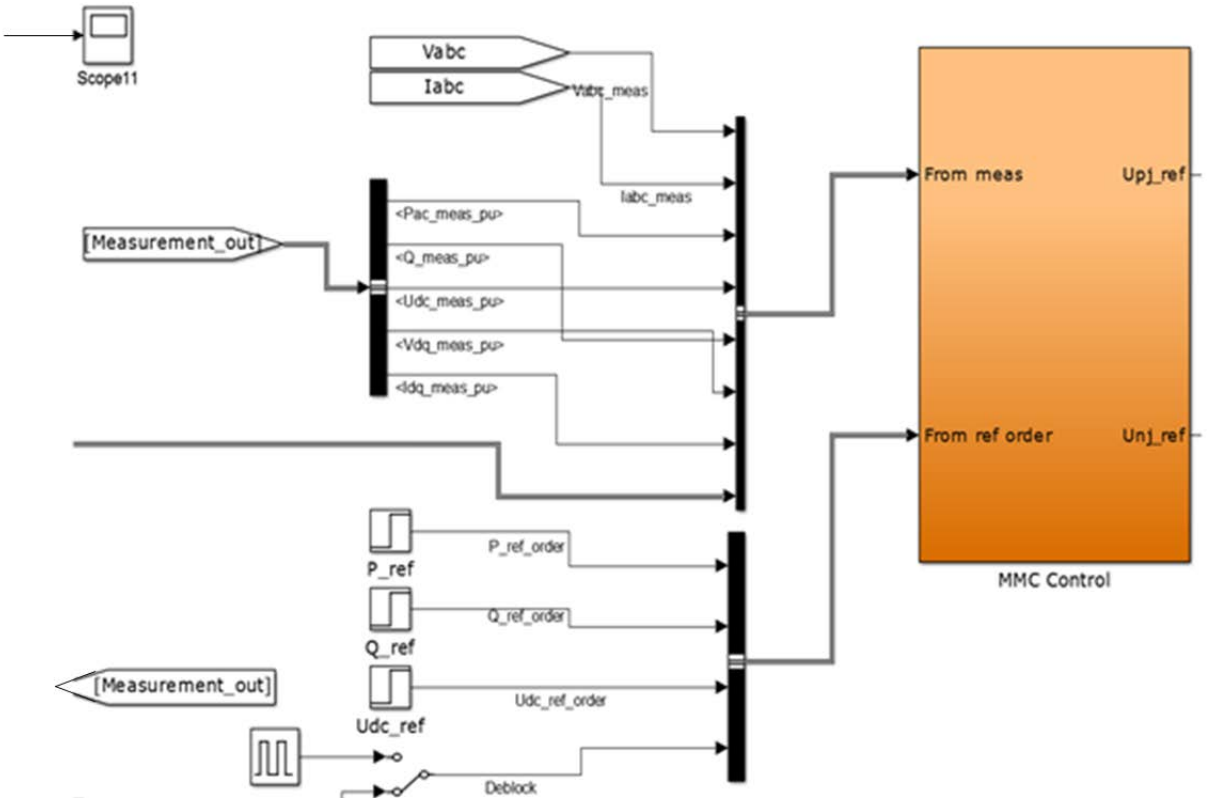


Figure 10 MMC controller block

3.2 Simulation results

The converter start-up, reactive and active power step, and DC load step scenarios are simulated in this section. The corresponding results are provided.

3.2.1 Start-up sequence

The purpose of the start-up sequence simulation is to evaluate the interaction between the MMC converter and control during the restart after the system fault event occurs. This is bearing in mind the reference to Figure 3 which envelopes the entire series of events from fault occurrence followed by detection, isolation leading to eventual fault-free system restoration within the 8 ms target. The simulation conducted in this case only contains one MMC converter behavior. Research planned for the near future will focus on the multi-MMC restart sequence.

In the start-up stage, the MMC converter needs to establish DC voltage as soon as possible, and meanwhile keeping the phase current and branch current within the safe operation limits. Although, this safety margin is not discussed in this subsection as it is an engineering issue and depends on the capacity of semiconductor devices and other passive components. In other words, the safe margin issue is the electric stress that the devices can undertake. The capacitor is pre-charged and then gate pulses are sent to the power cell to set up the DC voltage. The DC voltage reference is set to 800 V.

Tuning of the PI controller of the DC voltage control loop is relatively tedious, because there is more than one PI control loop, the DC voltage control is the outer loop while the fast current control is the inner

loop. Figure 11 shows the start-up of the DC voltage which takes 60ms to reach to the steady-state operation voltage. The time can be tuned by changing the limit of *d-q* current. Shorter time means larger charging current.

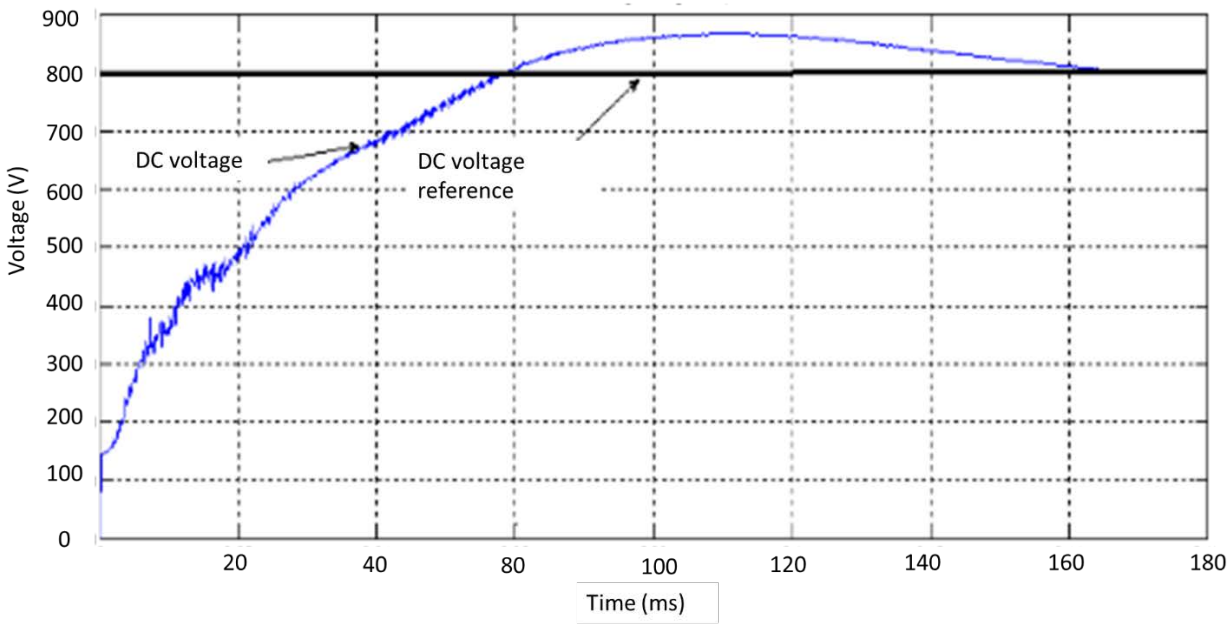


Figure 11 DC voltage Step 1.0 p.u.(start-up)

3.2.2 Active power step change

After the start-up sequence simulation is performed, a resistive load of 8 Ω is connected to the DC side and the controller is put in active power control mode to simulate the active power step. Due to the excessive time requirement for initialization, the cell voltage is pre-set to 133.33 V to indicate the capacitor has been already fully charged. The 1.0 p.u. active power step is simulated. The results of active and reactive power are given in Figure 12. The active power step changed at 0.02s, and initial oscillation is observed in the first 0.03s after the reference is released. This is because of the lack of implementation of direct control of DC voltage and cell voltage control. Furthermore, it will take longer to stabilize the DC voltage of the fast DC voltage control and cell voltage control is not implemented.

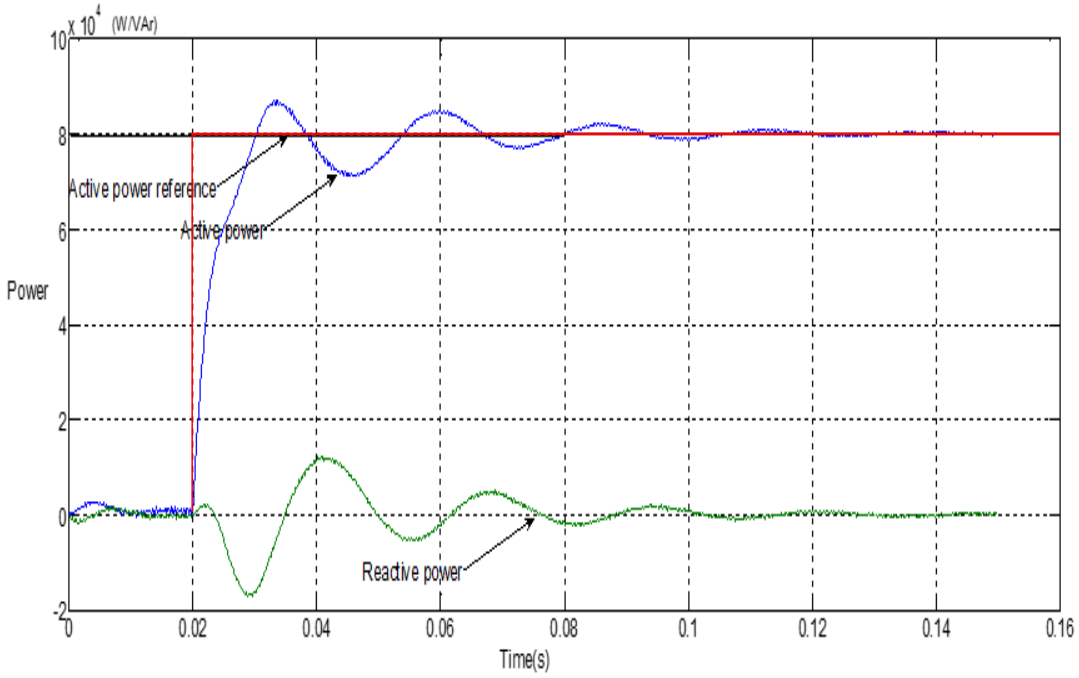


Figure 12 Active power step change to 1.0 pu

The system response does not have power oscillation when the cell voltage is well controlled. The similar simulation process is done under clamped cell voltage condition and the result is given. Figure 13 shows the response for that case.

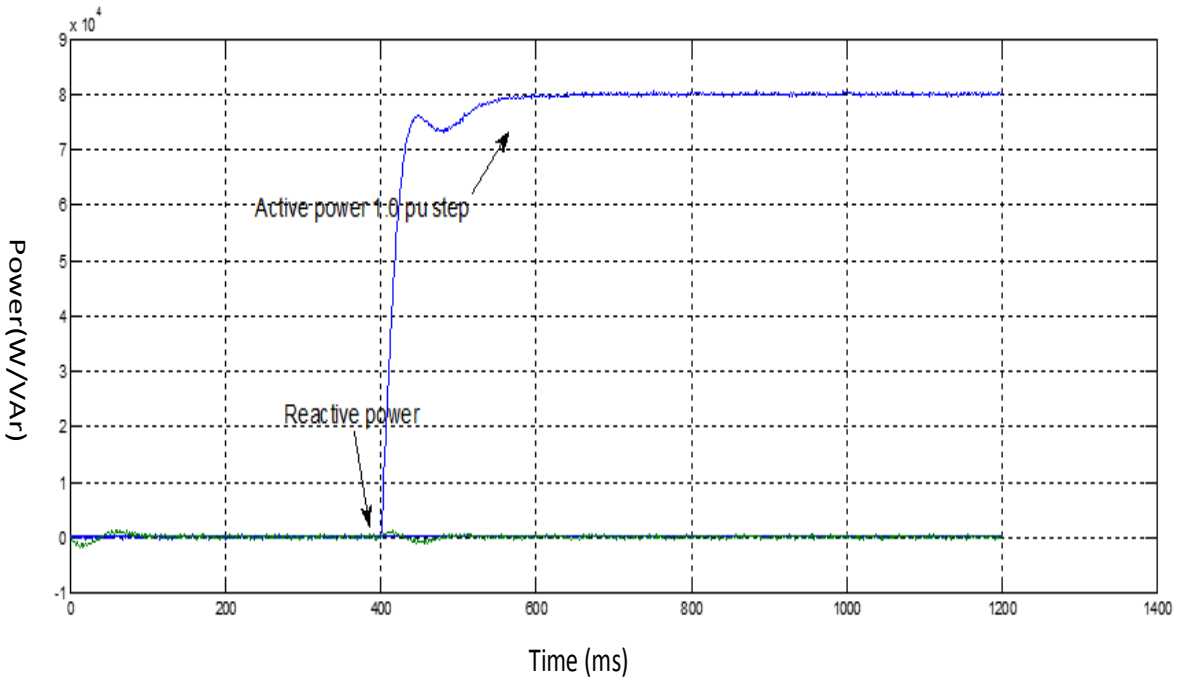


Figure 13 Active power step with clamped cell voltage

3.2.3 Reactive power step change

In this simulation scenario, 100% p.u. reactive power step reference is given to verify the control strategy. The result is given in Figure 14. Similarly, the reactive power step change response has the same oscillation compared with the active power step change.

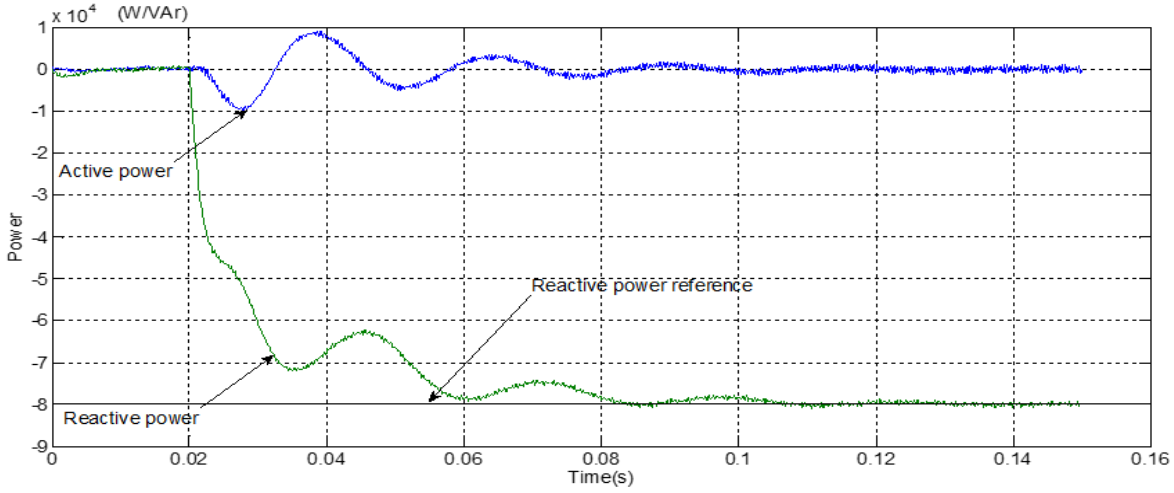


Figure 14 Reactive power step 1.0 p.u.

3.2.4 DC load step change

In order to test the U_{dc} response under fault conditions, a DC load is used to connect to the DC side to create a DC current step. The step-change has been applied when the converter is in the steady state with

800 V DC voltage, and the controller is in DC voltage control mode. A pure resistance (8 ohms) is used in this case. We connected the load to the DC side at 0.05 s after the simulation was started. The U_{dc} response is given in Figure 15.

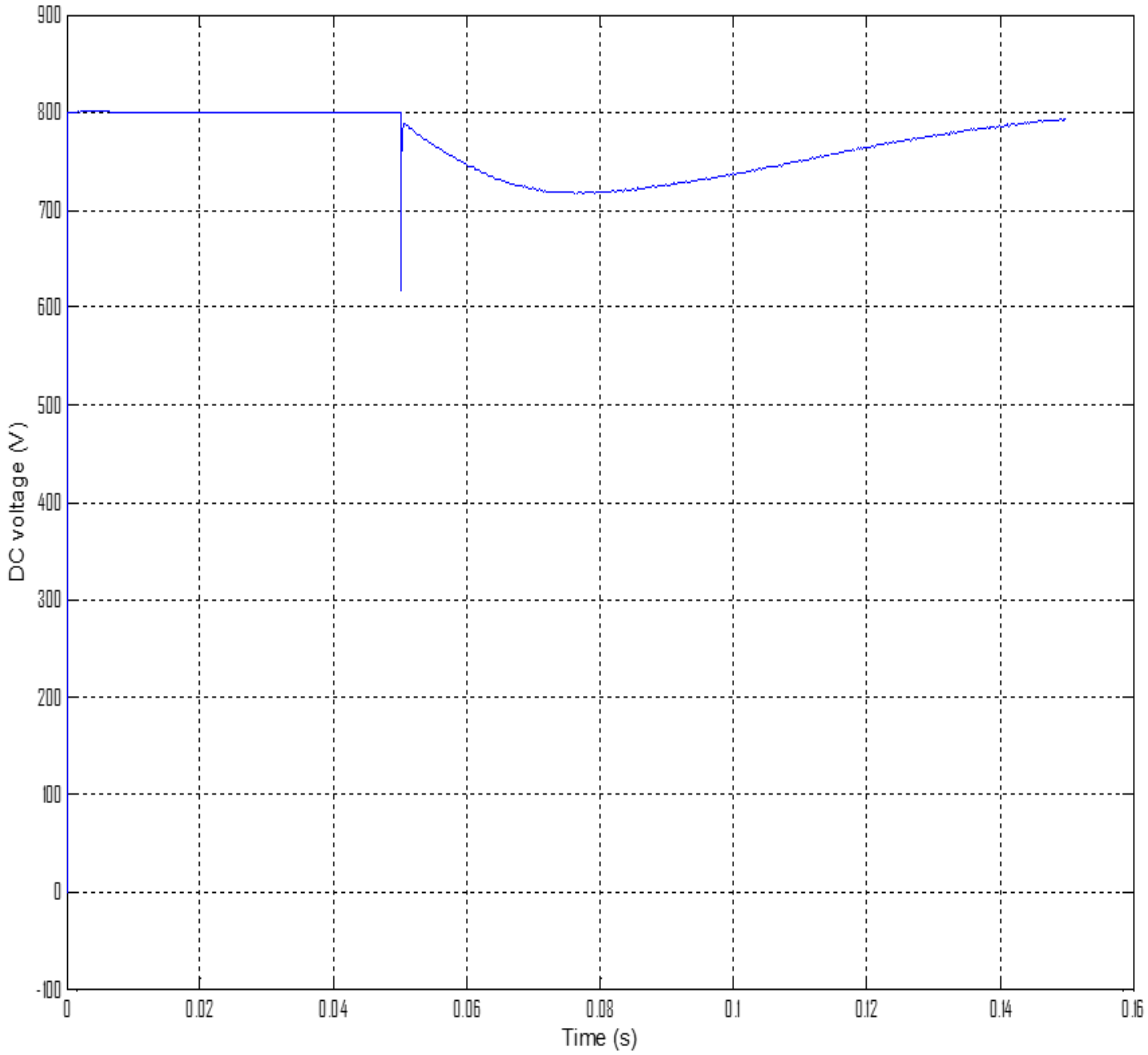


Figure 15 DC voltage under DC load step change condition

The DC voltage dropped to 630 V when the load step happened at 0.05s (Figure 16), and the current jumped to 100 A since it is a resistive load, the current change is instantaneous. If an inductor is introduced in the DC side, the current will not increase abruptly. The controllable DC side is difficult to realize because of controller response to the DC voltage drop will take a long time.

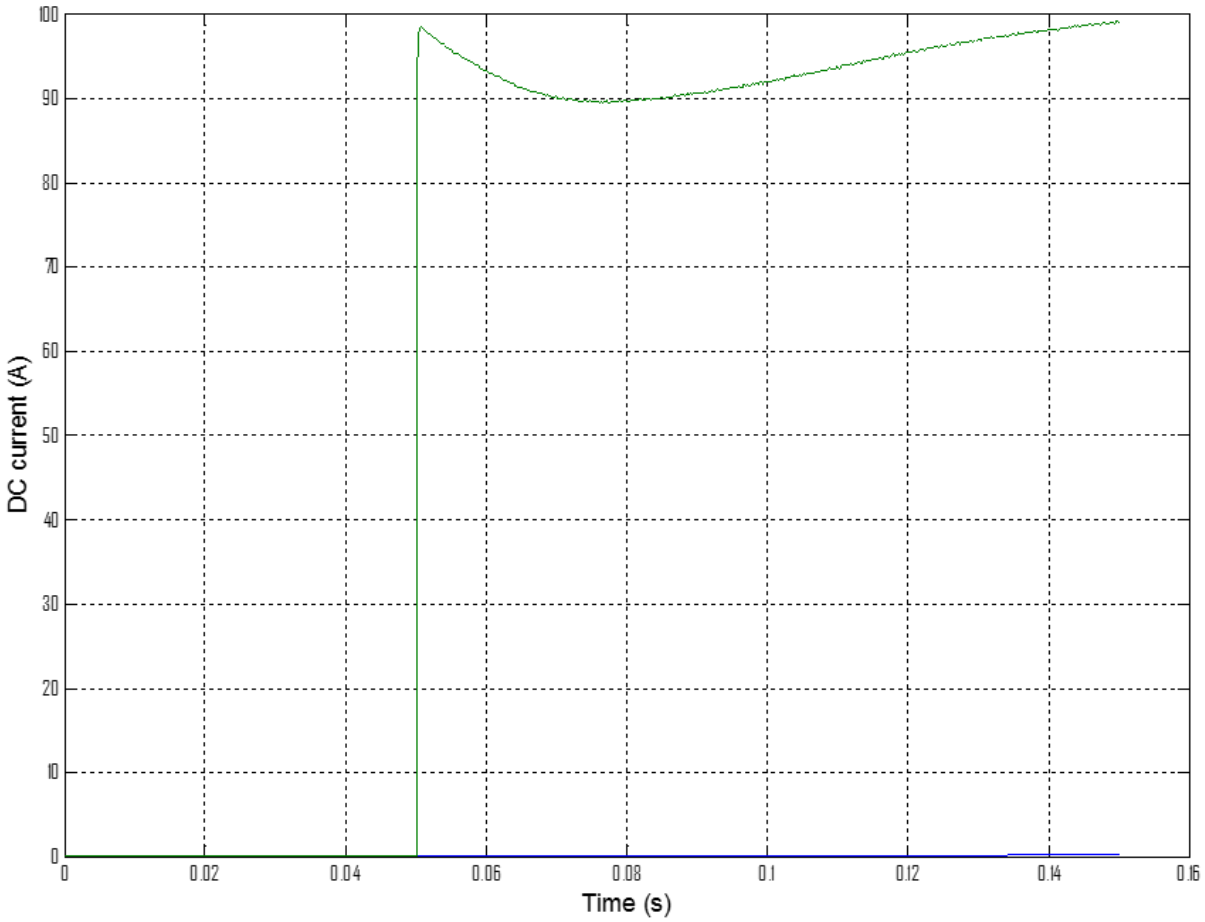


Figure 16 DC current under DC load step change

4 DC-DC CONVERTER CONTROL AND COORDINATION STUDIES

Section 1 and 2.2.5 underpinned the importance of coordination between the MMC converters (at source) and the downstream DC-DC converters (at loads) during fault events. Successful coordination would enable a fault ride through capability. Section 3 explained analysis and simulations pertaining to MMC converter control and integration for the MVDC network. This section highlights the approach adopted at FSU to investigate DC-DC converter control strategies that seek to enable coordination between MMC converters and zonal converters.

4.1 Initial analysis

The preliminary study of the control strategy of DC/DC converter in fault ride-through has been completed. Following points identify the various aspects of this work:

- **Control strategy –** A novel fault-ride-through control strategy is proposed
- **Energy storage –** The energy storage requirement for powering the load during fault period is calculated and the parameter of converter hold-up capacitor is designed

4.1.1 DAB converter topology

The topology of DC/DC converter is Dual active bridge (DAB) shown in Figure 17 and has the following advantages:

- Galvanic isolation, safety and voltage matching
- High frequency operation, high power density and small input capacitor
- High efficiency, soft switching of devices
- Suitable for high power applications
- More control degrees of freedom to achieve multiple functions such as wide input voltage range, current limiting capability and soft start-up

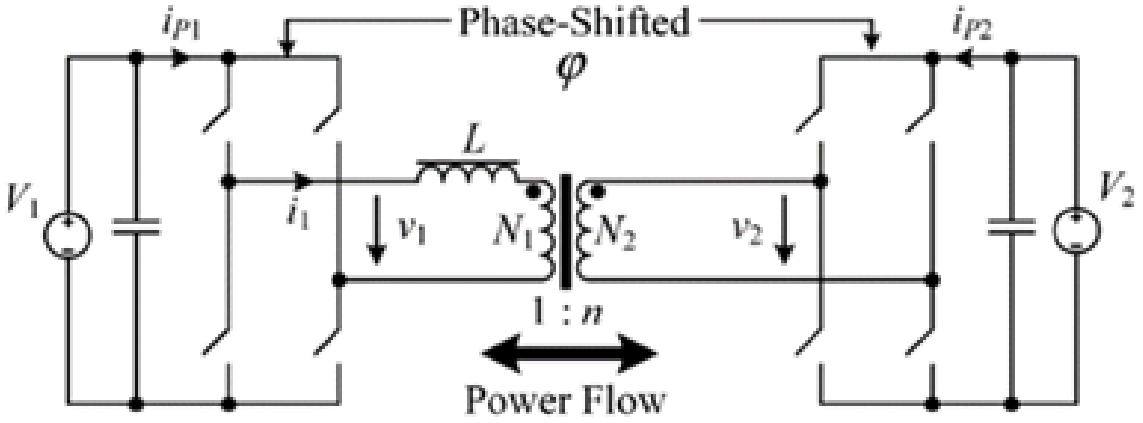


Figure 17 The DAB topology [13]

In conventional phase shift control, the secondary H-bridges of the DAB are modulated with a fixed duty cycle and active power is controlled by phase shift between these two waveforms. The phase shift control can be explained using the phasor diagram and the equivalent circuit shown in Figure 18. As shown in the phasor diagram, the maximum voltage drop on the inductor L is limited by the current rating of power semiconductors. Therefore under fixed duty cycle d, there exists a maximum phase shift angel φ_2, which

further limits the range of equivalent input voltage v_1. If the input voltage is lower than that range, an over-current protection or under voltage protection will be triggered.

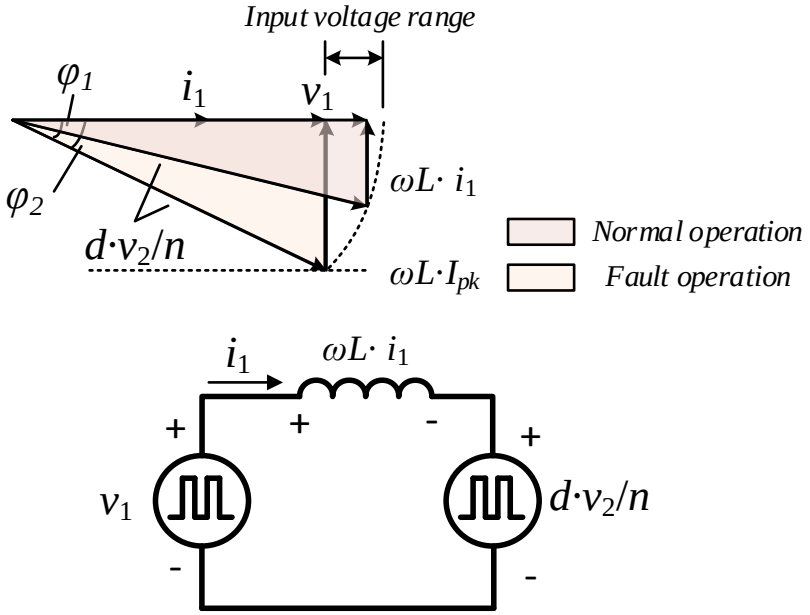


Figure 18 Phase shift control of DAB converter

4.1.2 Control strategy

In this research, a phase shift & duty cycle control is proposed. The operation principle is explained using Figure 19, and the control block diagram is shown in Figure 20. As in Figure 18, when input voltage dropped below a pre-set level, fault operation mode will be enabled, under which the duty cycle is also regulated based on the geometric relationship shown in the phasor diagram.

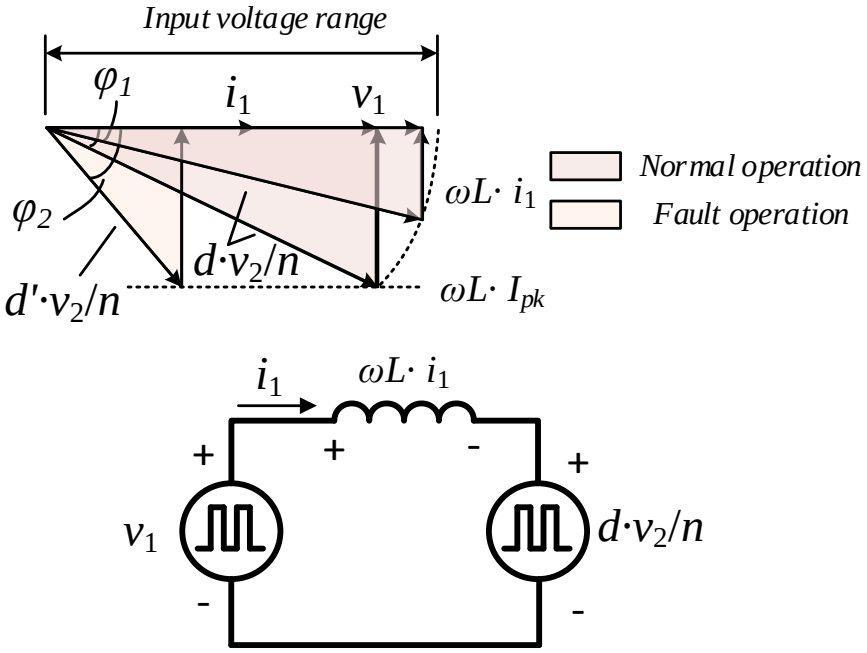


Figure 19 Phase shift and duty cycle control of DAB converter

Control block of proposed control strategy is shown in Figure 20. A fault detection logic is used to switch between the two operational modes, by detecting the value and slope of filtered input voltage. Compared with conventional control in Figure 18, the proposed control strategy has following features:

- Can operate at a very wide input voltage range – There is no theoretical limitation on input operation range, however, the nonlinearity of control plant at very low input voltage should be considered and further investigated.
- Capable of providing energy to the load during fault condition – This feature will slow the decrease of voltage drop at the load side. With proper design, this feature can provide an uninterruptible power supply (UPS) function for zone load.

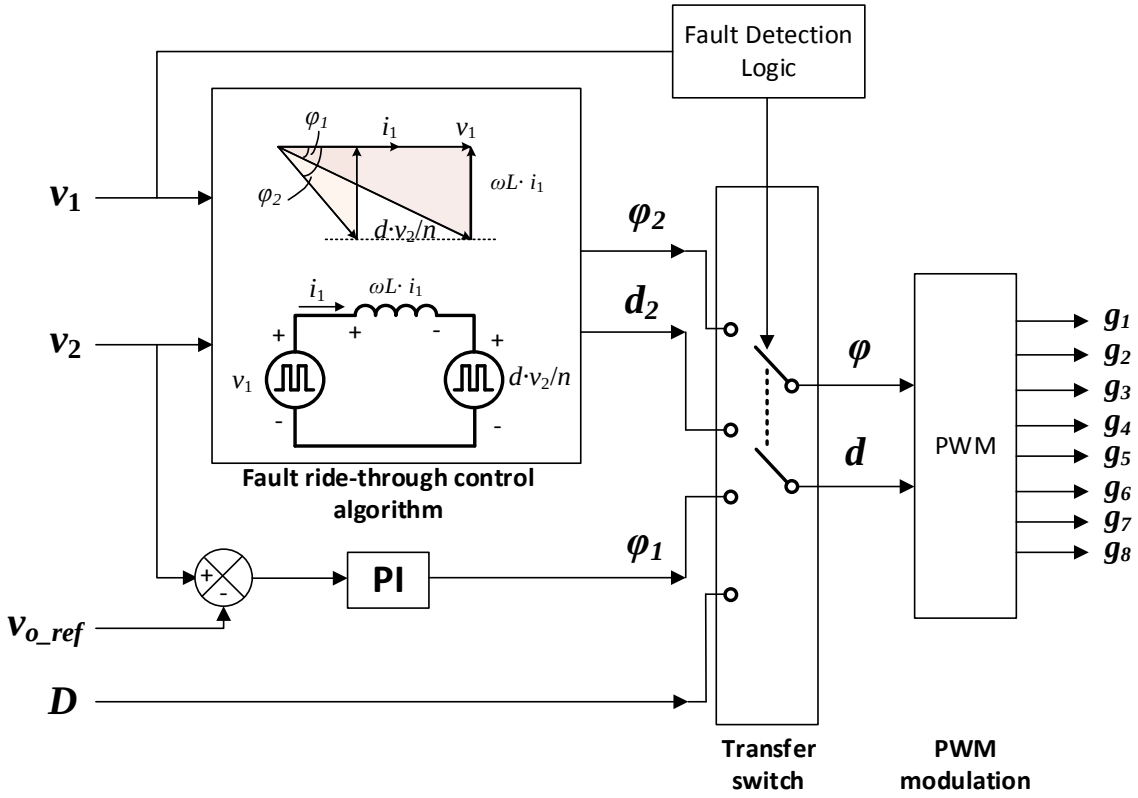


Figure 20 Control block of proposed control strategy

4.1.3 Energy storage requirement

Although the control strategy shown in Figure 20 is able to keep the converter operational during fault period, another dimension of the fault ride-through is to keep powering the crucial zone load. To achieve this purpose, certain amount of energy is required, besides advanced control of converter. Basically there are two potential energy source during fault period, one is the energy left in the DC bus (the input of the converter), and the other is the energy stored in the output capacitor. Both have been analyzed in our research.

The energy stored in the DC bus is calculated using equivalent circuit shown in Figure 21. Following assumptions have been made:

- All the energy stored in the capacitors and inductors can be extracted
- There is no resistive loss during the transfer of energy
- The converter efficiency is 100%

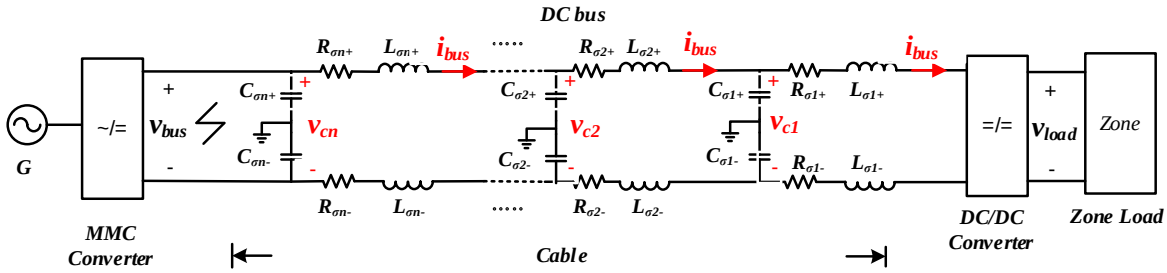


Figure 21 DC bus equivalent circuit

Since none of above assumptions can be fully realized in practice, the result based on assumptions from Table 4 is the most optimistic one.

Parameter	Value used
i_{bus}	625 A
v_{bus}	6 kV
p_o	3.75 MW
$cable\ length$	227 ft.
$Distributed\ capacitance, C_\sigma$	43.4 nF
$Distributed\ inductance, L_\sigma$	33.21 μH
$Distributed\ resistance, R_\sigma$	3.25 $m\Omega$

Table 4 Assumptions for values for a load zone

We calculated the maximum hold-up time using energy stored in the DC bus based following equations:

$$E_L = \frac{1}{2} i_{bus}^2 (L_{\sigma 1+} + L_{\sigma 2+} + \cdots + L_{\sigma n+}) + \frac{1}{2} i_{bus}^2 (L_{\sigma 1-} + L_{\sigma 2-} + \cdots + L_{\sigma n-}) = i_{bus}^2 L_\sigma$$

(a)

$$E_C = \frac{1}{2} (v_{C1}^2 C_{\sigma 1+} // C_{\sigma 1-} + v_{C1}^2 C_{\sigma 2+} // C_{\sigma 2-} + \cdots + v_{C1}^2 C_{\sigma n+} // C_{\sigma n-})$$
$$\leq \frac{1}{2} v_{bus}^2 (C_{\sigma 1+} // C_{\sigma 1-} + C_{\sigma 2+} // C_{\sigma 2-} + \cdots + C_{\sigma n+} // C_{\sigma n-}) = \frac{1}{4} v_{bus}^2 C_\sigma$$

(b)

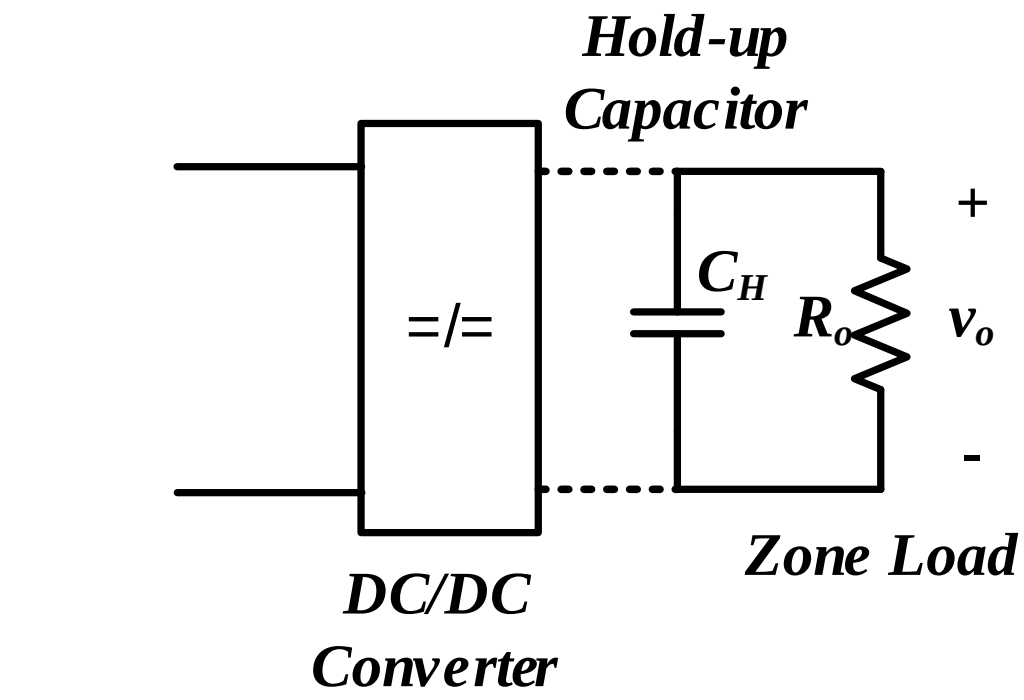
Equation 1 (a) Cable inductance-energy (b) Cable capacitance-energy

The total energy that can support a zone in the network is the sum of that for the individual filter elements, which when divided by the power, gives us the corresponding time value.

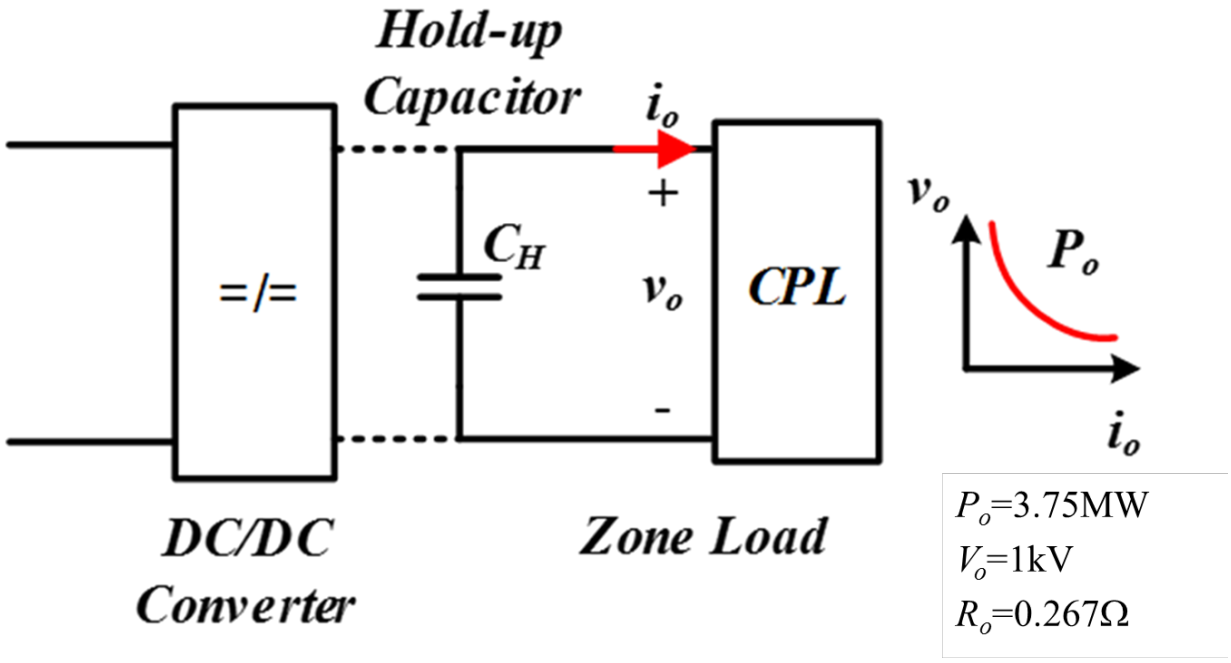
$$Hold\ up\ time = \frac{E_L + E_C}{p_o} = \frac{i_{bus}^2 L_\sigma + \frac{1}{4} v_{bus}^2 C_\sigma}{p_o}$$

Equation 2 Hold up time corresponding to parasitic capacitance and inductance

The result shows that the maximum hold-up time is 3.56 μs, which is too small and hence insufficient to support the load through the fault period. Therefore powering the load using an output capacitor as an alternative could then be considered. Figure 22 (a) shows the equivalent circuit of using output capacitor to power the constant power load (CPL). For $p_o = 3.75\ MW$ and $v_o = 1\ kV$, considering $t = 4ms$ as the required hold-up time, voltage drop at the load side for different hold-up capacitors is calculated as shown in Figure 22 (b).



(a)



(b)

Figure 22 (a) Equivalent circuit of using output capacitor to power the load (b) Equivalent circuit showing a CPL and associated parameter values used

The following energy balance equation could be used to determine the value of the hold-up capacitor C_H.

$$Energy\ balance:$$
$$\frac{1}{2}C_H(v_o^2(t) - V_o^2) = -P_o t$$

gives in p.u.,

$$v_{o(p.u.)}(t) = \frac{\sqrt{V_o^2 - \frac{2P_o t}{C_H}}}{V_o}$$

Equation 3 Voltage per unit, in terms of hold up capacitance

Inserting maximum hold up time as $t = 4ms$ and $v_o(t) = 0.1V_o, 0.5V_o, 0.9V_o$, we obtain the values for capacitor C_H shown in Figure 23.

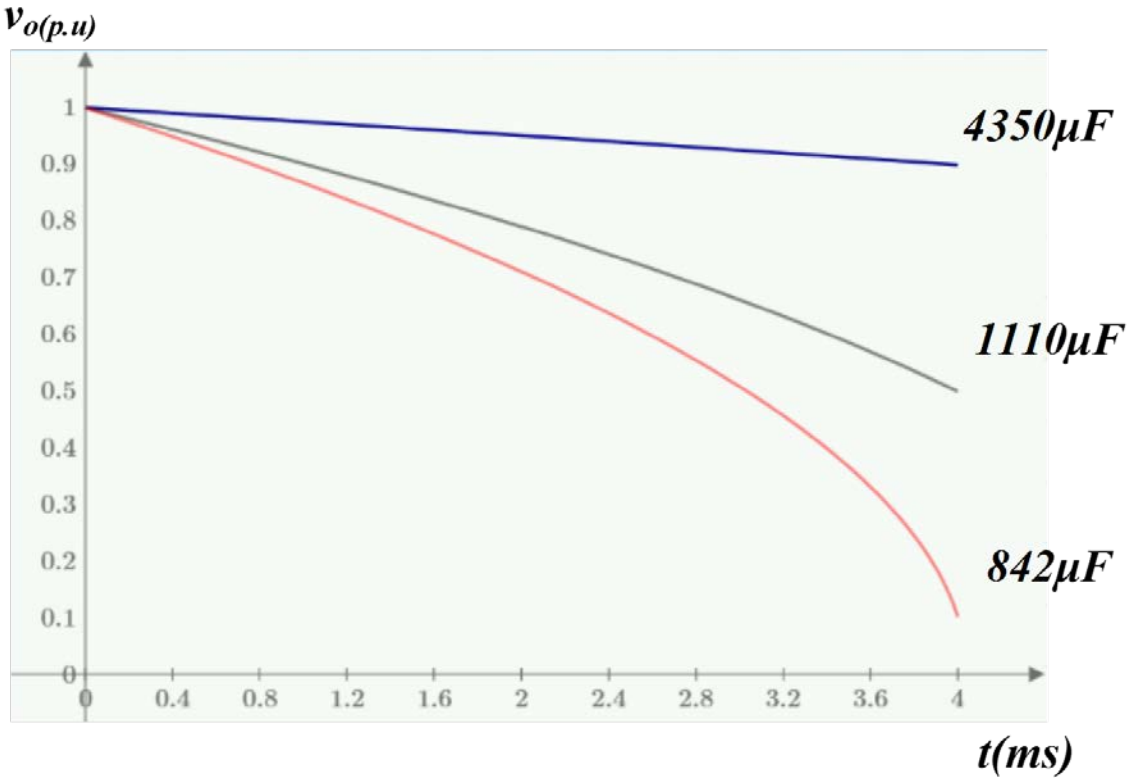


Figure 23 Hold up capacitor values for maximum hold up time of 4 ms

Figure 24 shows the corresponding plots to visualize the relation between capacitor value and voltage drop.

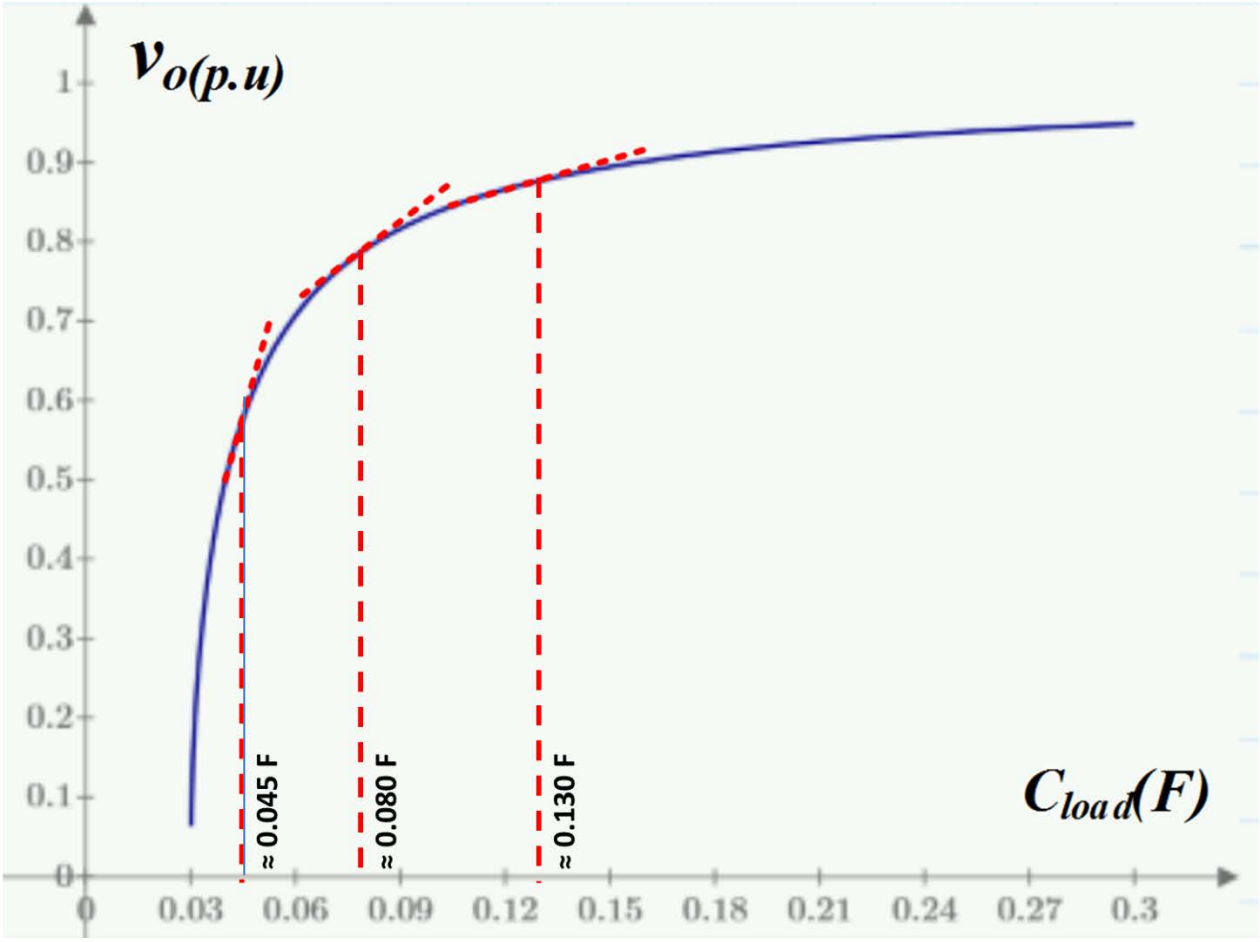


Figure 24 Required hold-up capacitance versus load side voltage drop.

As can be seen from Figure 24, larger capacitance will result in smaller voltage drop. However the relationship is not linear, which means over certain value of capacitance, increasing capacitance will be less efficient, and also not economic. The red dotted lines are tangents to various points of the curve showing the particular capacitance for the corresponding value of voltage drop. Such a curve is helpful to select the value of the hold-up capacitor and supplements to Figure 23. Based on the calculations shown, we can conclude that 0.03 F-0.09 F for the hold-up capacitor is a reasonable range of values. However, this capacitance is still large in the circumstance that there is a short circuit fault on the load side. Thus, the next stage of this research sub-task will be focused on:

- Analysis and simulation on the dynamic response of proposed fault ride-through strategy
- Modify the DAB topology so that it requires less capacitance in the output.

5 CENTRALIZED FAULT MANAGEMENT (CFM) BASED ANALYSIS

The previous 2 sections were dedicated to analysis of converters at the source side as well as load side. These studies focused on integration of MMC converters into the MVDC shipboard system and the coordination of downstream DC-DC converters inclusive of suitable control schemes for both. In general, this constituted studies at a device level to address the issue of fast system restoration after a severe fault event.

This section and section 6 are dedicated to the system or sub-system level analysis to deal with large scale interruptions. This section provides a summary of the work conducted within this specific research arena from a detailed Ph.D. thesis on the subject of CFM for MVDC systems [14].

The research into developing the proposed CFM approach consists of the following parts:

1. **Defining protection challenges** – An overview of possible protection challenges in the MVDC system that need to be taken into consideration to design the proposed CFM system.
2. **Proposing a CFM approach for MVDC** – A more centralized fault management approach that considers the aforementioned challenges related to MVDC protection. The approach is based on zone division and adapted percentage differential protection methods. It is highly adaptive to smart grids with different structures and operating conditions. It also minimizes the need for coordination of the different zones.
3. **Characterizing communication requirements for CFM** – A complete set of models built for the three types of CFM systems in order to characterize the performances of the CFM systems. These models will be able to describe accurately the operating performances of the CFM systems and provide benchmarks for protection designs of the proposed approach.
4. **Developing a generic design guidelines for the CFM approach** – By defining four detailed protection design procedures, we developed a generic design guideline of how to the CFM approach to distribution system of different structures and operating features.

5.1 Overview of CFM research at CAPS-FSU

This section and its subsections underscore the various aspects of work conducted within the proposed CFM for protection of MVDC shipboard systems research arena. As mentioned before, a PhD thesis [13] is the primary outcome of this research.

A CFM system is composed of a CFM unit with protection program, remote sensors and associated communication work. As shown in Figure 25 the MVDC system is partitioned into a number of protection zones for the purposes of fault localization and isolation. There are (or more, depends on the size of the MVDC system) two CFMs encompassing the entire representative MVDC network, each manages multiple zones with differential schemes. When a fault occurs, the differential schemes will indicate if the fault is inside or outside its range. Thus the location of the fault can be determined.

This research uses an Adapted Percentage Differential Protection (APDP) scheme for fault identifications in the CFM program. Compared to the traditional differential protection scheme, the major distinction with the APDP scheme is based on instantaneous value of sample points, rather than the RMS value, so that the CFM system can potentially be used for the MVDC system with a fast speed of a sub-cycle.

Figure 26 shows the detail arrangement of a unit within a CFM system, the remote sensor (DQ) are distributed at the disconnect switches of the network, where they measure current and send the digitized

data to their corresponding CFM unit. In this way, a CFM system is perceived to provide protection for a large portion of the MVDC system, by executing protection schemes for all the zones in its area.

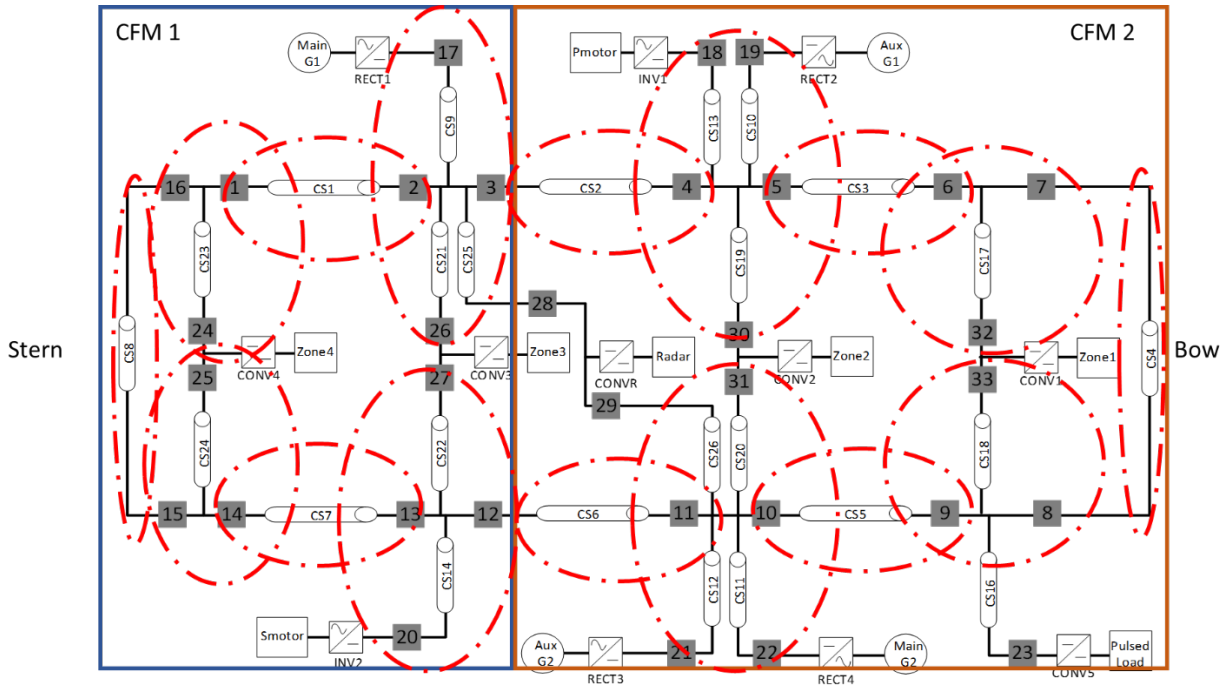


Figure 25 CFM proposed for representative MVDC shipboard power system

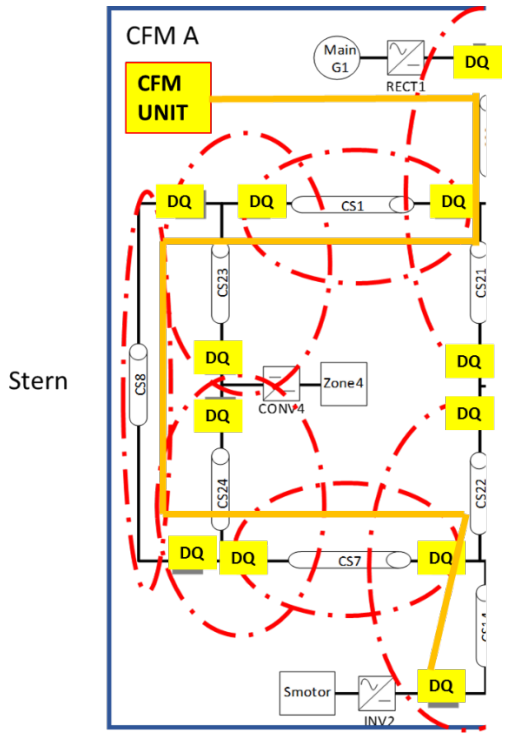


Figure 26 Detailed view of a CFM unit

The subsections to follow shed further light on the CFM approach.

5.1.1 Protection structure of the proposed CFM approach

In contrast to the traditional protection approaches that are constrained by the local relays, the CFM approach applies a new protection structure, which is composed of a combination of digital data acquisition and real-time communication. In the new structure, multiple CFM systems are deployed to manage a smart grid by processing the same sensor information, and thus to provide protection redundancy and to ensure overall system reliability. The new structure is expected to enable the development of a new generation of protection technology, which will facilitate the rapid design and implementation of a highly adaptable protection approach for smart grids of both AC and DC types. A representative diagram of using such a multiple-CFM based method is shown in Figure 27.

5.1.2 Three types of CFM systems and performance models

As discussed in [6], there are two types of communication topologies: the typical serial topology and the new parallel topology. The serial topology is mature and effective; however, the parallel topology performs better for a large number of slaves also referred to as an analog merging unit (AMU). For CFM system connection in smart grids, either the line connection or star connection could be used. The line connection is relatively simple and easy for a CFM system, while the star connection offers better survivability and flexibility for protection applications.

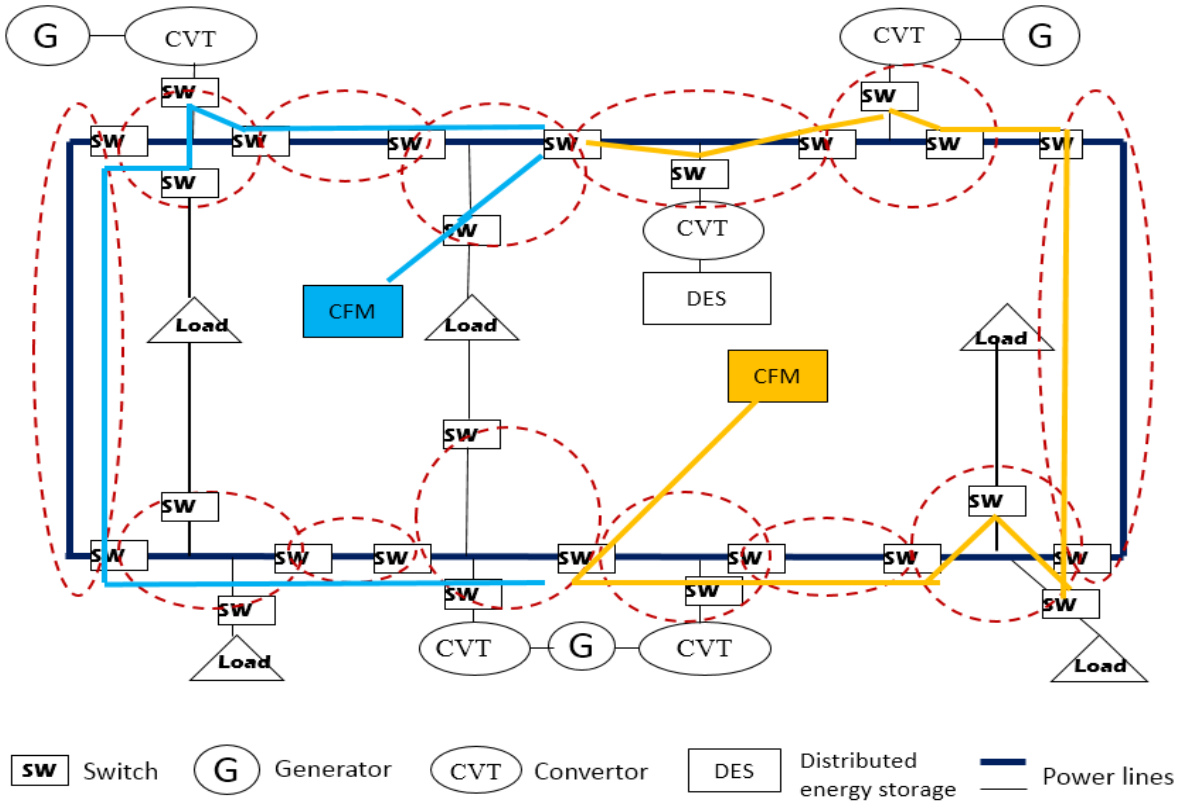


Figure 27 Protection concept of the CFM approach for smart grid protection

Thus, there are three types of CFM systems possible for the proposed CFM approach, as shown in Figure 28:

A. Line connection in serial topology.

B. Star connection in serial topology.
C. Star connection in parallel topology.

It is necessary to build complete models for the three types of CFM systems followed by calculating the performance characteristics of the three models in MATLAB. This is followed by using a network simulator, the OPNET software, to validate the CFM models. The OPNET simulation results show that the models are accurate in analyzing the performance of the CFM systems. Figure 29 shows the CFM cycle time (in μs) for different number of slaves in a CFM system. In the figures, the solid lines represent the results of OPNET simulation, while the dashed lines represent the results of MATLAB calculation. We can see that the maximum differences between OPNET simulation results and MATLAB calculation results are: 2.8% for the type-A system, 5.0% for the type-B system, and 7.4% for the type-C system. These results validate the accuracy and correctness of the models.

For the three types of CFM systems: the type-A system is advantageous for smart grids of small scale; the type-B system provides a backup way to implement the star connection, but it sacrifices some performance; the type-C system has better performance for smart grids of large scale.

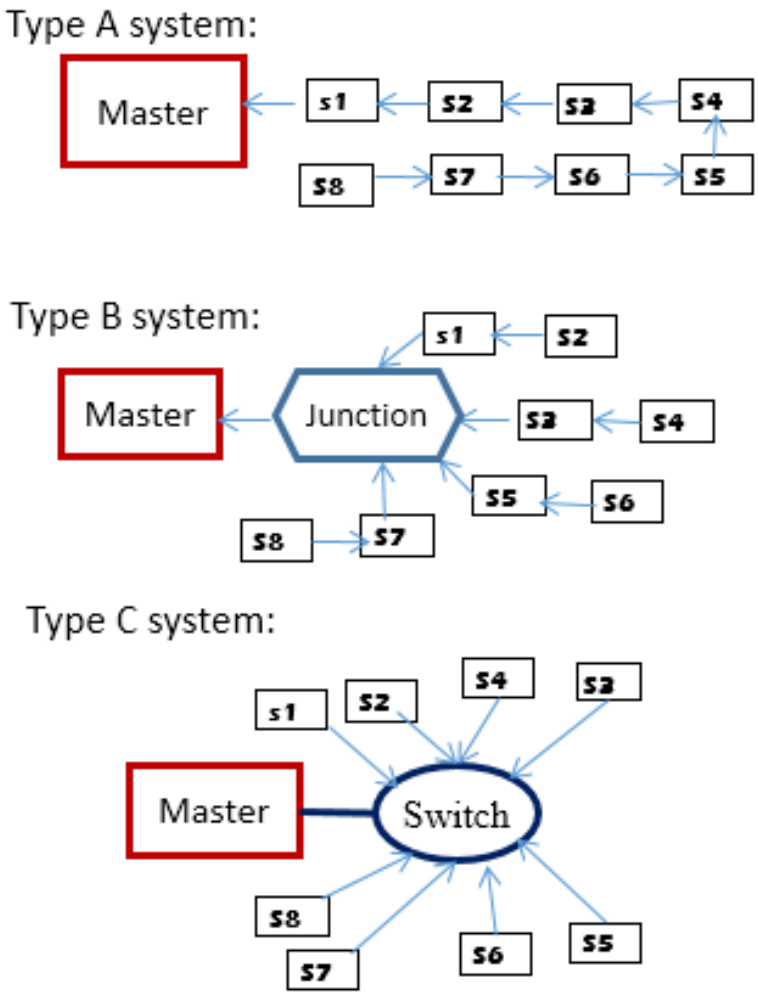


Figure 28 Three types of CFM

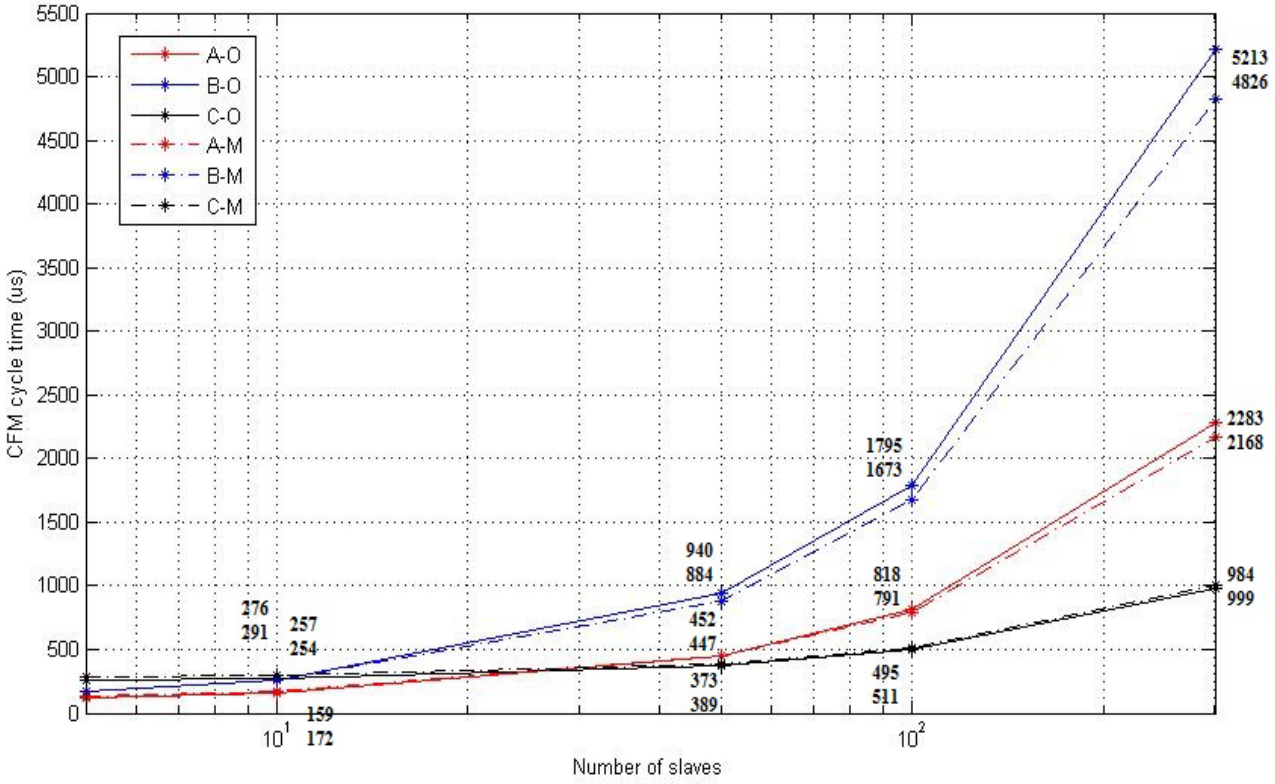


Figure 29 Result comparison of slave numbers: OPNET and MATLAB [14]

5.1.3 CFM for MVDC shipboard applications: Building a demo.

For a complete evaluation and validation of the CFM approach, a demonstration CFM system with 12 inputs, and then apply the CFM system to an HIL test-bed of a looped smart grid on a RTDS system is proposed to be built. The RTDS system is a real-time power system simulator, and can provide electro-magnetic transient analog signals to facilitate the interface with our CFM system hardware. Moreover, the RTDS system allows us to verify the proposed CFM system in a real-time environment that is very close to practical operation conditions of the MVDC system.

The closed-loop connection diagram is shown in Figure 30. A simplified MVDC simulation running on the RTDS and the demonstration CFM system with protection functions already exists at CAPS. Two systems with cables are connected in such a way that the AMUs in the CFM system can measure signals from the RTDS, and then send the data to the CFM unit. The real-time analog signals, which reflect the simulation results of the MVDC system, become available to the CFM unit. The CFM unit monitors the smart grid based on this data and sends out a trip signal when a fault is determined. It is important to note that the MVDC simulation is from an earlier version of the project which is still implemented with circuit breakers.

The zonal division strategy is then applied to the MVDC simulation. The circuit mapping and zone division (or zoning) are shown in Figure 31, where it is shown that the CFM covers four protection zones (PZ) of the MVDC looped (PZ 1-4). However, the zoning aspect is highly flexible: one can move the PZ4 to PZ0 in the CFM system without make any modification to other 3 zones. The dashed-line circles indicate the division of the zones, which usually have circuit breakers at the edges, so as to isolate faults in a zone.

After this step, configuration of the 4 zones in the CFM unit with the DQ nodes, according to the graphic mapping in Figure 31 is carried out. The protection program is built in Labview software and its control panel is shown Figure 32. The control panel consists of 4 zone-status lights and 4 monitoring scopes for PZ1 and PZ2. The 4 zone-status lights are located on the top of the control panel, they highlight the protection status of the CFM system in real-time. Initially, the 4 lights are off. At the detection of a fault in any of the 4 zones, the corresponding zone light will be turned on. The 4 monitoring scopes, display details of operating conditions for PZ1 and PZ2 in real-time. Notice that, the upper scope shows the current value in the zone, and the lower scope shows the status of the trip signal. When a fault occurs at PZ1, the CFM unit identifies the fault in zone 1 in approximately 4ms. Then, the status light for zone 1 is turned on and a trip signal is generated. The magnitude of fault currents are limited to 3 times of the rated current, and the waveform of the currents are highly distorted. The CFM is able to successfully identify the fault in the zone 1, and the non-faulty zones (2, 3, and 4) operate without interruption.

As mentioned earlier this proposed CFM approach is based on the APDP scheme and calculation of instantaneous sample points. Therefore, the CFM approach is universally applicable to smart grids that have different operating features. Faults at PZ1 and PZ2 are tested with various operating conditions of generators in service. The experimental results are shown in Table 5 where the CFM system clearly distinguishes the faulty zones under different operating conditions. Testing was done for the performance of the CFM under dynamic conditions of generator switching on/off. The promising results demonstrate that the proposed protection system achieves a satisfactory accuracy and reliability which also identify the adaptability of the CFM approach.

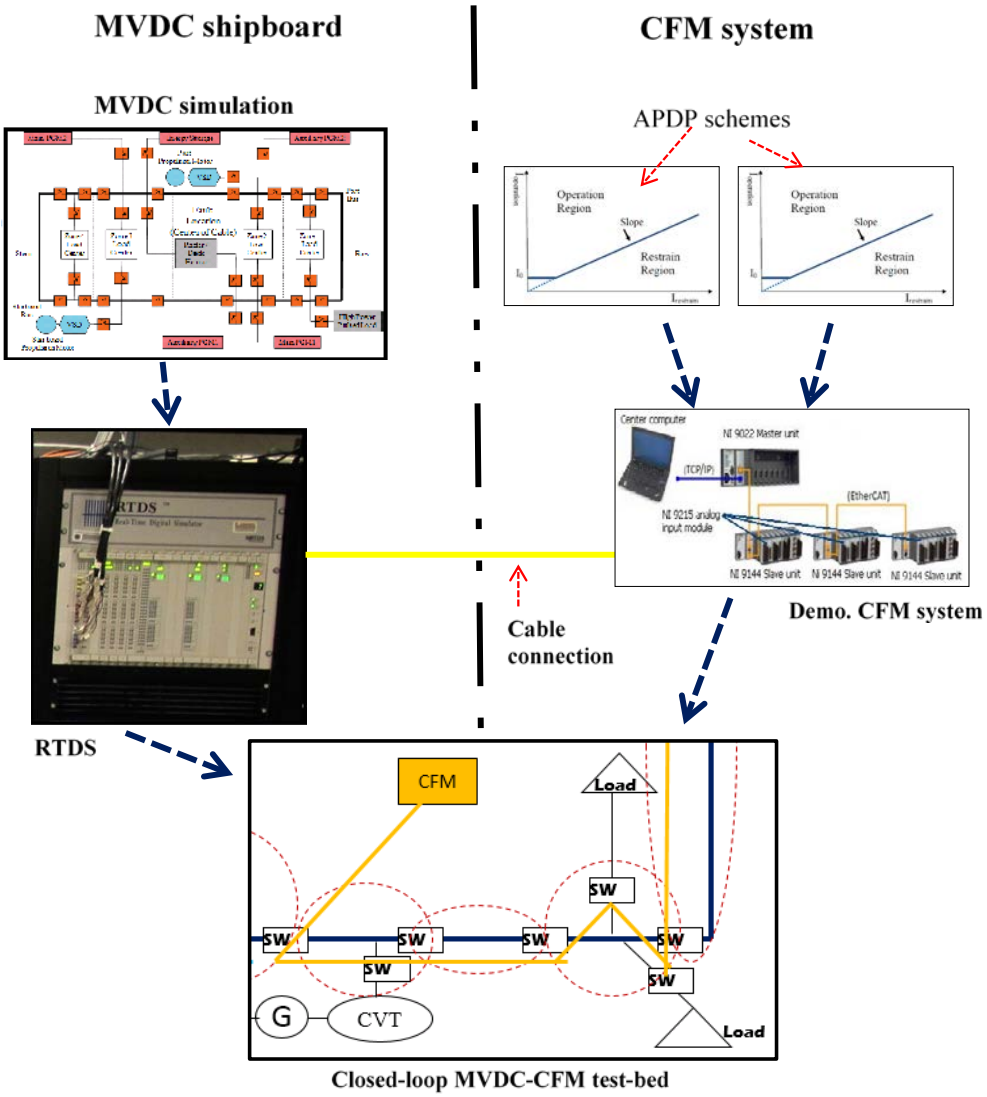


Figure 30 The MVDC-CFM closed loop testbed

Fault location	Generators in service	PZ1	PZ2	PZ3	PZ4
PZ1	4	Y	N	N	N
PZ1	3	Y	N	N	N
PZ1	2	Y	N	N	N
PZ2	4	N	Y	N	N
PZ2	3	N	Y	N	N
PZ2	2	N	Y	N	N

Table 5 Faults and protection results of the HIL testing

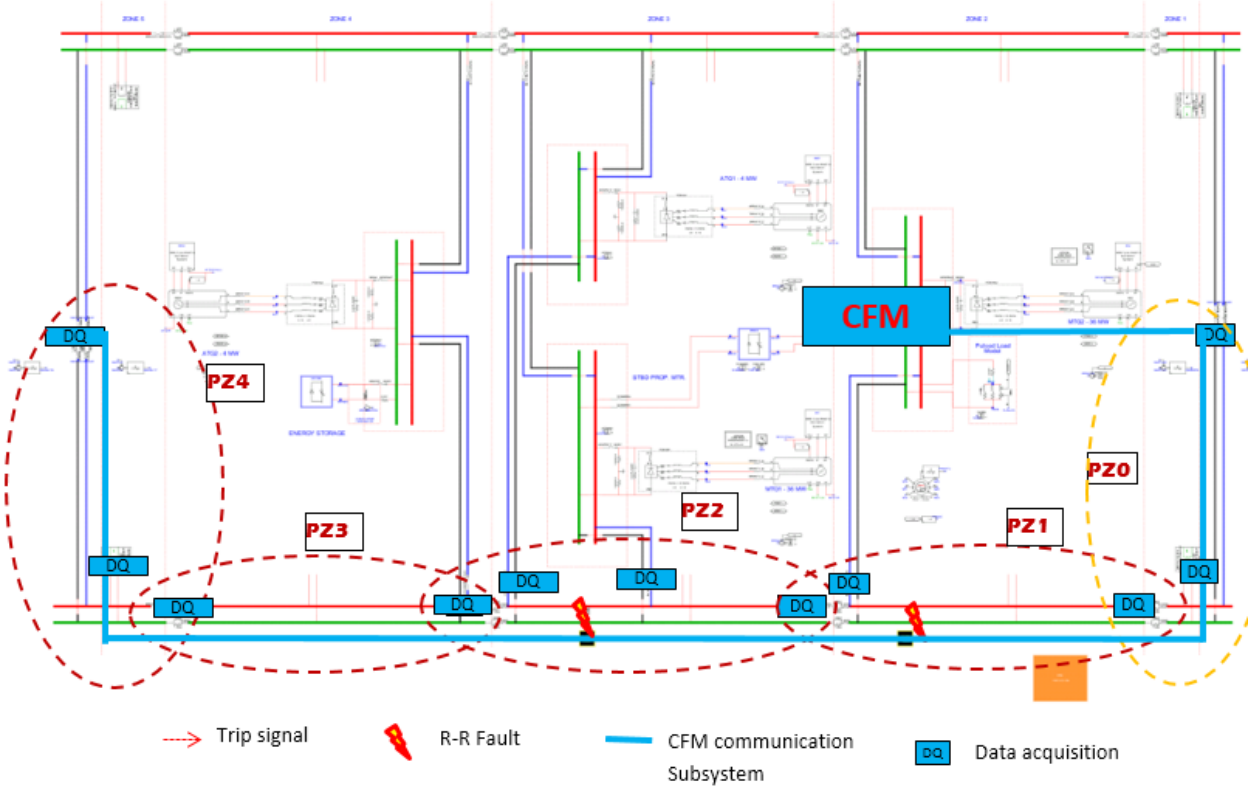


Figure 31 The MVDC-CFM protection ranges

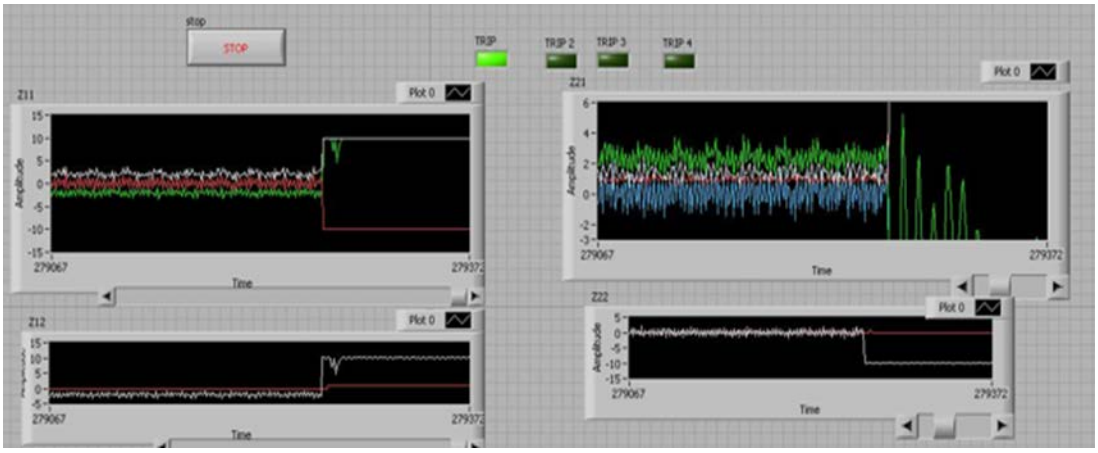


Figure 32 Labview control panel

5.2 Summary of outcomes and planned future work

This section provided details of the research conducted under the CFM approach for protection of the MVDC shipboard system. Following is the summary of the major advantages of this approach which is a promising outcome.

1. **Adaptability** – The usability of the conventional protection approaches are highly constrained by the structure of MVDC system. Whenever the structure changes, the entire protection system

needs to be reconfigured. The proposed CFM approach is designed to be adaptable to different structures, even for shipboard systems in both AC and DC types.

2. **Ease of configuration** – In the conventional protection approaches, we may be able to use multiple relays to protect the MVDC system, but the coordination between the relays will be very difficult to achieve. In the proposed CFM approach, since there is only one centralized protection device, no coordination is needed between protection devices. Thus the protection functions of the smart grid can be accomplished by configuring only one device.
3. **External control capability** – The PEDs, which inherently provide additional control capability, are largely integrated into smart grids. Therefore, the CFM approach is expected to make full use of PEDs' controllable feature on protection control, such as convertor controls for fault interruption, and switch controls for fault isolation. In this way, the CFM approach also provides feasibilities for satisfying the demand of system-level protection controls in the smart grids.
4. **Fast protection speed** – As the protection scheme of the CFM approach is derived from the differential protection scheme, which is one of the fastest protection schemes, the CFM approach inherently has a fast protection speed compared to conventional protection approaches. Currently a 4 ms protection response is achieved for the demonstration CFM system.

A comparison of general attributes of conventional protection approaches and the proposed CFM approach is listed in Table 6.

Conventional protection approaches	Proposed CFM approach
Distributed protection concept	Centralized protection concept
Different protection designs for smart grids are required	One highly adaptive design for smart grids of different structures and operating features
Protection zones are fixed	Protection zones are flexible
Many relays distributed throughout the smart grid	One CFM covers a large portion of a smart system
Simple, mostly analog sensor-to-relay connection structure	Sensor information shared on a CFM unit, communication subsystem required
Not applicable to AC/ DC grids	Feasible for AC/DC grids
Multiple protection schemes work together: coordination problems	Uniform protection scheme: no coordination necessary
Elaborate configuration for protection devices	Facilitates easy and standardized configuration for one CFM unit
Limited post-fault control capability	Uninterruptible load supply capability

Table 6 Comparison of protection approaches

For the future work, the primary tasks to focus on are:

- More accurate modeling of the processing delay
- Hardware implementation of a full CFM system
- Full protection HIL test for MVDC shipboard
- External control functions used with CFM

6 LOCAL FAULT MANAGEMENT (LFM)

Reiterating the main objective of this research task being to develop a method for protecting MVDC distribution systems against short circuit faults, this section highlights current work conducted at USC, built upon previous research related to coordinating the action of controllable power supply converters with the action of bus tie switches and mechanical contactors [3]. An appropriate detection algorithm was designed optimally that permits both a reliable detection of faults and coordination between the different elements involved in the protection of the system. Also, this protection method was simulated at medium voltage and megawatt level in addition to conducting experiments on a scaled low voltage hardware testbed.

Focus of the work under Task 4.2.1 at USC is to develop a Localized Fault Management (LFM) scheme that adheres to the goal of addressing the challenge of coordinating electronic power converters and mechanical contactors to rapidly isolate short circuit faults while maintaining continuity of power to loads. The primary objective of the LFM is to serve as a back-up system to the previously mentioned CFM approach.

Under the LFM scheme, the source power converters independently enter into current-limiting mode as soon as they recognize a fault condition rapidly de-energizing the distribution bus. The bus segmenting contactors autonomously open or not based on their local interpretation of time-to-trip curves as functions of apparent equivalent circuit resistance, also called “distance relay”. After the fault is cleared, the bus will be reconfigured via mechanical contactors, and the system will be

LFM is anticipated to allow converter and contactors to coordinate to provide fault protection for MVDC distribution systems even in the event of communication failures. The MVDC fault protection sequence

includes LFM initially reacting to fault locally due to the fact that all the measurements are taken locally without remote communication time delay. This in turn implies that in the event of the CFM rendered inoperable due to communication failures, the LFM will function as a final backup for the whole system. In this manner, the LFM related work at USC is aimed to complement as well as supplement the CFM research at FSU.

Table 7 summarizes the fundamental differences between the CFM and LFM approaches.

Characteristic	CFM	LFM
Operating speed	Aimed at 2 ms	Aimed at 10-20 ms
Devices	2 or 3 CFM devices	Multiple LFM devices
Coordination	No coordination needed among the CFM devices	All LFM devices need to be coordinated
Algorithm	Adapted differential algorithm	Adapted impedance algorithm
Communication media	A dedicated communication system needed	Simple, direct analog wiring

Table 7 Differences between CFM and LFM

This section describes the various aspects that constitute the overall LFM approach and individual strategies. The following 3-step process summarize the general fault protection methodology which is adopted for the specific LFM application:

1. **Zero reset** – After a fault is identified, the current limit set points of converters that feed the affected bus should be reset to zero.
2. **Isolation of faulted branch** – As soon as the initial discharge fault current decays to the rated opening current of the mechanical contactor or bus tie switch (but before the current actually reaches zero) appropriate contactors are actuated to reconfigure the system thus segregating the faulted section. This operating mode takes advantage of the forward voltage of the low-current inter-contact arc to more-rapidly drive the system current to zero. But during this time, the current is small enough so as not to damage the contactor.
3. **Re-energizing the system** – After the current is driven to zero and any other contactors are repositioned to effect any desired system reconfiguration, converter set points are reset so as to re-energize the system.

6.1 Fault detection and coordination approach within LFM

The time evaluation of apparent resistance was considered here as the characteristic that provides a fast and effective method for detecting and identifying short circuit faults in MVDC power distribution systems. This method allows source converters, bus tie switches, and mechanical contactors to use only local measurements when discerning whether or not to trip into fault isolation mode. The process is divided into two distinct steps,

1. **Terminal resistance calculation** – Each converter is equipped with a controller that is capable of measuring current and voltage, and calculating the value of the equivalent resistance at the output terminals at each sample time from the relationship in Equation 4,

$$R_n(t) = \frac{V_n(t)}{I_n(t)}$$

Equation 4 Terminal resistance

Where;

$$V_n = voltage\ value\ after\ filtering\ and\ discretizing$$
$$I_n = current\ value\ after\ filtering\ and\ discretizing$$
$$R_n = equivalent\ terminal\ resistance\ of\ device\ 'n'$$

2. **Threshold resistance calculation** – The measurement is then used by the controller's decision algorithm that provides the converter with a current limiting reference or an enabling signal. When the converter recognizes an equivalent resistance lower than a pre-defined threshold, it goes into current limiting mode bringing the current down to a minimum value. The converter stays in current limiting mode until the equivalent resistance returns above a pre-defined threshold after a pre-defined time delay. The resistive threshold for fault detection R_{th} has to be smaller than the equivalent resistance corresponding to the heaviest load that the system is designed to supply (system rated load), as shown in Equation 5,

$$R_{th} = \frac{{V_r}^2}{P_r}$$

Equation 5 Threshold resistance

Where;

$$V_r = rated\ voltage$$
$$P_r = rated\ power$$
$$R_{th} = resistive\ threshold\ for\ fault\ detection$$

A similar fault detection algorithm is present in the controller of each contactor that segments the DC bus and each contactor between DC bus and loads as shown in Figure 33. In this case, the decision-making algorithm has multiple statuses due to the fact that contactors in different locations have different priorities for opening and each contactor is allowed to open when the current value falls below its own rated safe opening current threshold. Since the contactor is not designed to open the prospective maximum fault current (as a circuit breaker would), each contactor is allowed to open only after the current falls below its rated opening current. In these conditions the contactors can open the remaining current without damage.

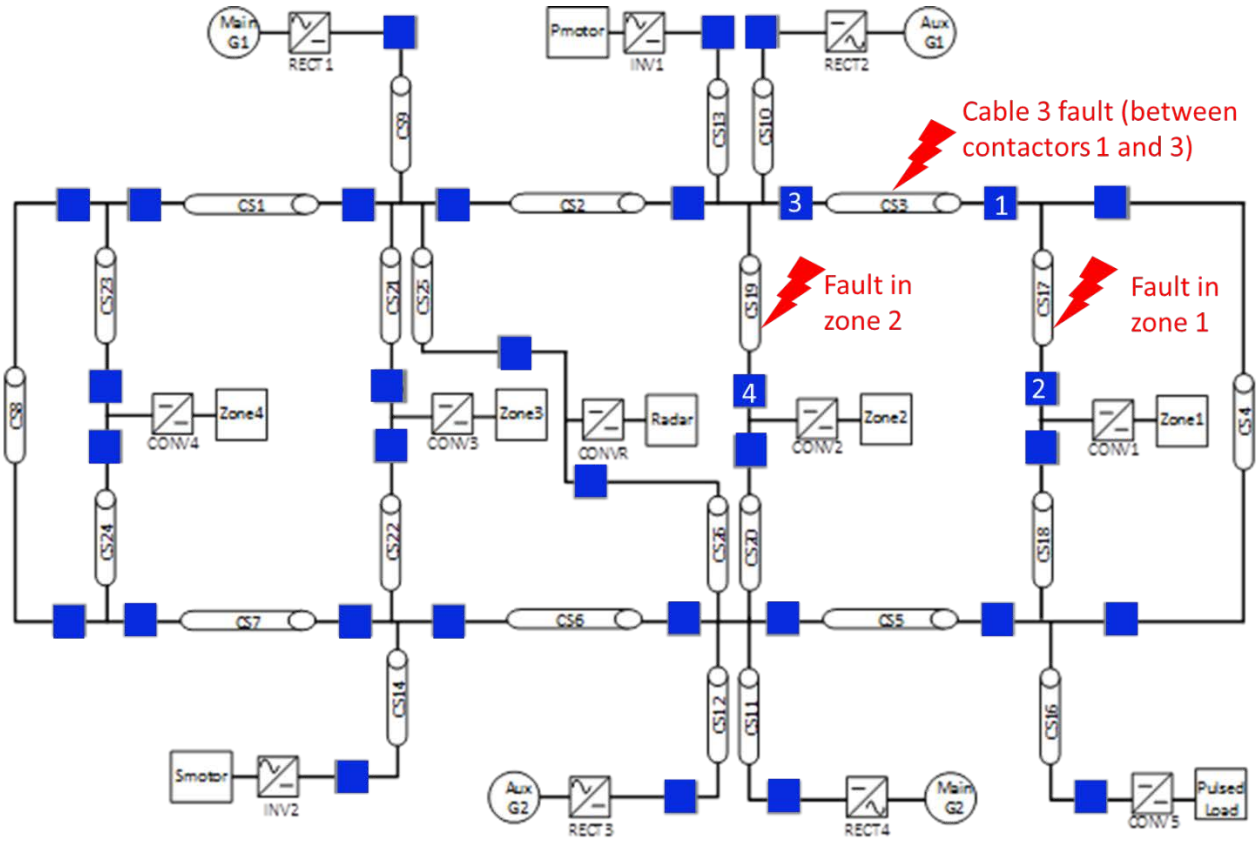


Figure 33 Multi-terminal zonal MVDC distribution system (blue squares are mechanical contactors)

6.2 Further development at USC

While this method has been experimentally proven for DC/DC converters in an open end ring bus system, it can also be applied to MMC AC/DC converters that interface AC sources to the DC close loop ring bus power system.

Both voltage and current measurement are carried out at each rectifier in order to calculate the real-time equivalent resistance at the terminals using equation (2).Also Considering the resistances of interconnection cables at the $m\Omega$ level, which are over a 1000 times less than the resistance at loads, they can be neglected when calculating equivalent resistance at rectifier terminals. In normal operation condition, due to the fact that all the loads are parallel-connected to the ring bus, equivalent resistance at rectifier 1 can be calculated using Equation 6,

$$R_{rec1} = \frac{{V_r}^2}{\alpha \times (P_{pmotor} + P_{smotor} + P_{pulse} + P_{radar} + P_1 + P_2 + P_3 + P_4)}$$

Equation 6 Equivalent resistance at rectifier 1

Where;

$$R_{rec1} = equivalent\ resistance\ at\ rectifier\ 1$$
$$\alpha = \%\ of\ power\ delivered\ from\ main\ generation\ unit\ 1\ to\ the\ whole\ system$$

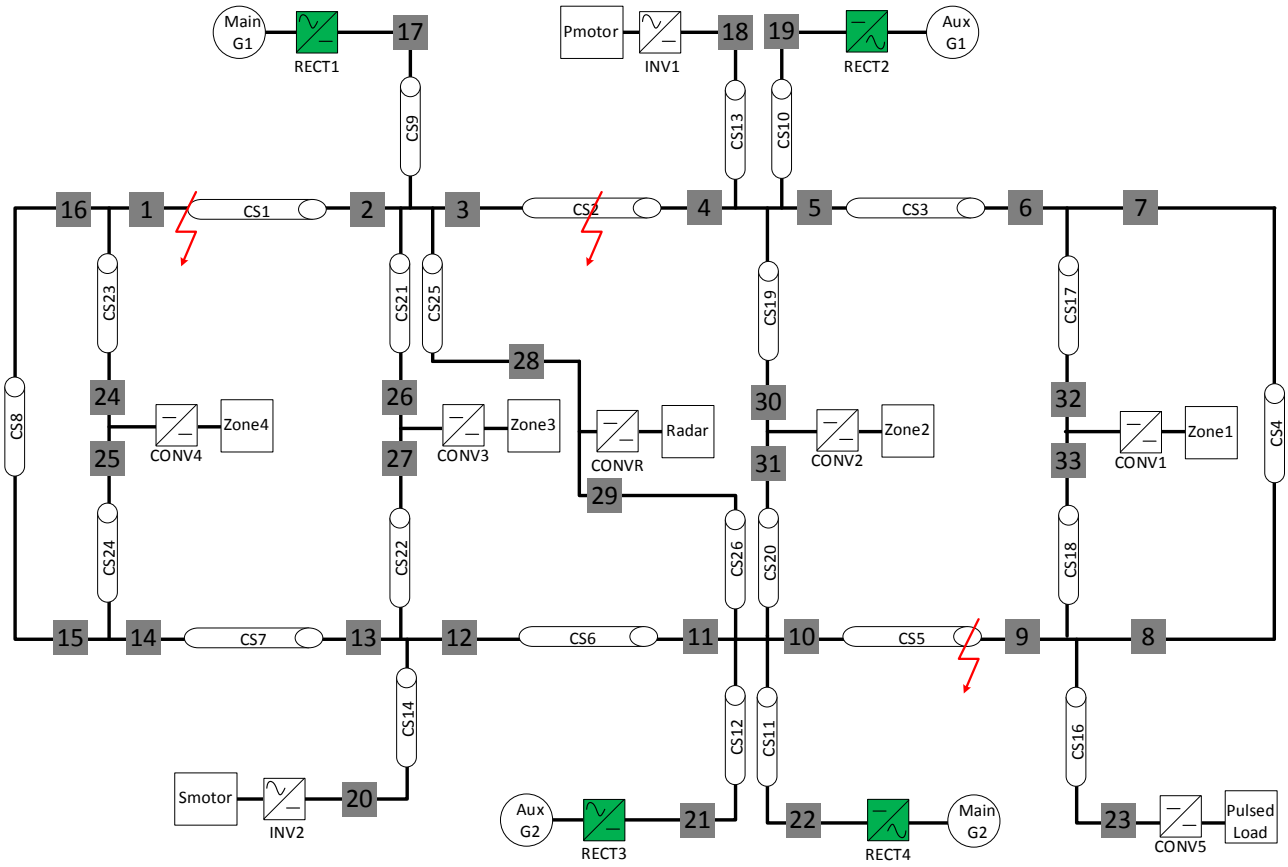


Figure 34 Fault event occurs at different locations along the close loop ring bus of MVDC Ship Power System.

For fault event occurs at different locations along the ring bus shown in Figure 34, according to the operation mechanism of Local Fault Management (LFM), all the rectifiers are expected to go into current-limiting mode once the fault event is detected by the algorithm, and followed by corresponding contactors in operation to cut off this fault segment from the system.

However in such low impedance (1 mΩ or less) fault condition, the short circuit fault provides much lower impedance route against other major loads (factor of 1000 times or lesser), while the impedance of cables and contactor on the ring bus are no longer negligible, so equivalent resistance at rectifier 1 can be calculated alternatively using Equation 7,

$$R_{rec1}{}' = \frac{1}{\alpha \times \left(R_{rec1_{cable}} + \frac{\left(R_{clockwise} + 2 \times R_{fault}\right)}{\left(R_{anticlockwise} + 2 \times R_{fault}\right)}\right)}$$

Equation 7 Alternative calculation of equivalent resistance at rectifier 1

Where;

$$R_{rec1\_cable} = resistance\ of\ rectifier\ 1 and\ cable\ connected\ to\ the\ ring\ bus$$
$$R_{CW} = clockwise\ sum\ of\ resistances\ from\ contactor\ to\ fault\ location$$
$$R_{ACW} = anticlockwise\ sum\ of\ resistances\ or\ cables\ CS2\ to\ CS8\ plus\ contactors\ 3\ to\ 16\ and\ contactor\ 1$$
$$R_{fault} = estimated\ fault\ resistance$$
$$R_{rec1\_cable} = output\ resistance\ of\ rectifier\ 1\ plus\ resistance\ of\ cable\ CS9$$
$$R_{anticlockwise} = resistance\ of\ cable\ CS1\ plus\ contactor\ 2$$

Therefore set the threshold value of characteristic resistance R_{th} at rectifier 1 to be above $R_{rec1}{}'$ but lower than R_{rec1} . When the measured resistance $R_n(t)$ is below this threshold value, rectifier 1 will go to current limiting mode. All the setup of other Rectifiers 2, 3 and 4 can follow the same procedure.

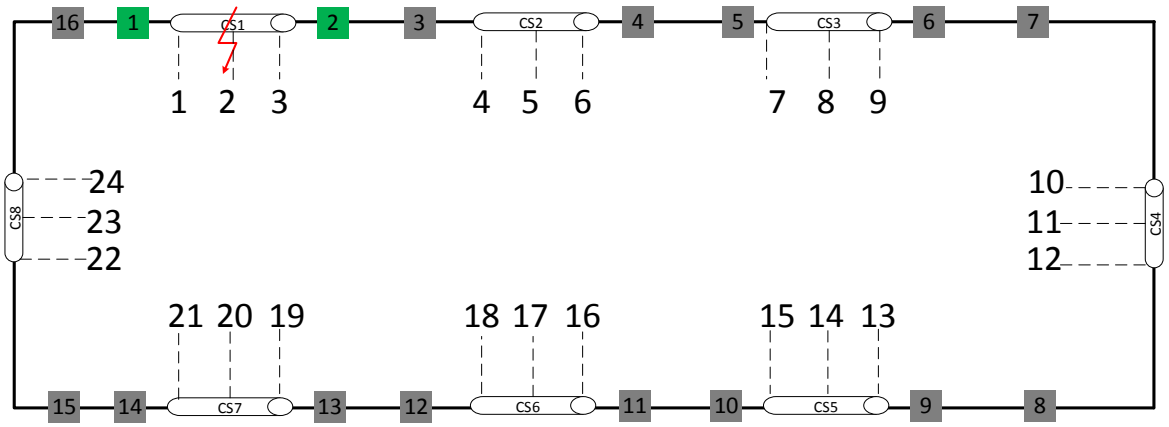


Figure 35 Contactors corresponds to fault at different locations along the ring bus of MVDC Ship Power System.

A similar fault detection algorithm is present in the controller of each contactor that segments the close loop ring bus as shown in Figure 35. In this scenario, each contactor needs to look at its own current and voltage status and simultaneously make the same decision – whether the fault is very near to me, or is it nearer to another contactor?. The ultimate objective for this fault protection algorithm is to make sure that the two closest contactors are assigned to cut off the faulted segment, while the remaining part of ring bus is still stay fully functional. For example, if low impedance fault occurs within cable CS1, contactor 1 and 2 will open to cut off cable CS1 from the ring bus while other contactors stay closed.

In normal operation condition, equivalent resistance R_n at contactor *n* could be calculated using Equation 8

$$R_{normal} = \frac{V_{r-ring}^2}{P_{contactor}}$$

Equation 8 Resistance under normal condition

Where;

$$V_{r-ring} = rated\ voltage\ at\ ring\ bus$$
$$P_{contactor} = power\ flow\ through\ contactor$$

In fault condition, equivalent resistance R_m at contactor *n* could be calculated using Equation 9

$$R_m = \frac{(R_{CW} + 2 * R_{fault})}{(R_{ACW} + 2 * R_{fault})}$$

Equation 9 Resistance under fault condition

Where;

$$V_{r-ring} = rated\ voltage\ at\ ring\ bus$$
$$R_{CW} = clockwise\ sum\ of\ resistances\ from\ contactor\ to\ fault\ location$$
$$R_{ACW} = anticlockwise\ sum\ of\ resistances\ from\ contactor\ to\ fault\ location$$

When fault happens at the ring bus, equivalent resistance measured at all the contactors will decrease significantly due to the contribution of low impedance fault, so that all the contactors sense a fault event. After that, each contactor opens or not based on the comparison of equivalent resistance measured and calculated through Equation 9 to its own fault tripping threshold value. It is obvious from Equation 9 that for contactors closest to the fault location, will exhibit lowest value of equivalent resistance at their terminals compared to those of contactors further away. Thus, this characteristic of equivalent resistance

responding to fault provides a possible way to cut off the correct and smallest portion of system during fault event.

Figure 36 shows equivalent resistance seen at terminals of contactor 1 and contactor 2 for different fault locations along the close loop ring bus system labeled in Figure 35. It is interesting to find that equivalent resistance seen at contactor 1 and contactor 2 will rapidly increase when the fault location is moving from close end to far end. For example in Figure 36, equivalent resistance at contactor 1 responds to fault at location 1, 2, 3, 22, 23, 24 is below 0.007 Ω, while above 0.013 Ω for fault at location 4~21. Therefore, this characteristic can provide guidance for adopting distance protection in such close loop ring bus MVDC system. The tripping threshold for each contactor can be properly set, so that it will guarantee the selectivity and robustness of contactor for fault protection. Take the case in Figure 36 for example, if the equivalent resistance seen from contactor 1 or 2 is above the upper boundary of tripping (0.012 Ω), contactor 1 or 2 will remain close, but if the equivalent resistance seen from contactor 1 or 2 is below the lower boundary of tripping (0.008 Ω), contactor 1 or 2 will definitely open to clear the fault. However, it also can be seen from the plot that for case in which fault happens at location 22~24, equivalent resistance at contactor 1will exhibit low equivalent resistance as well. Thus directional protection scheme will need to be integrated at the contactors in the future development in order to guarantee selectivity of protection.

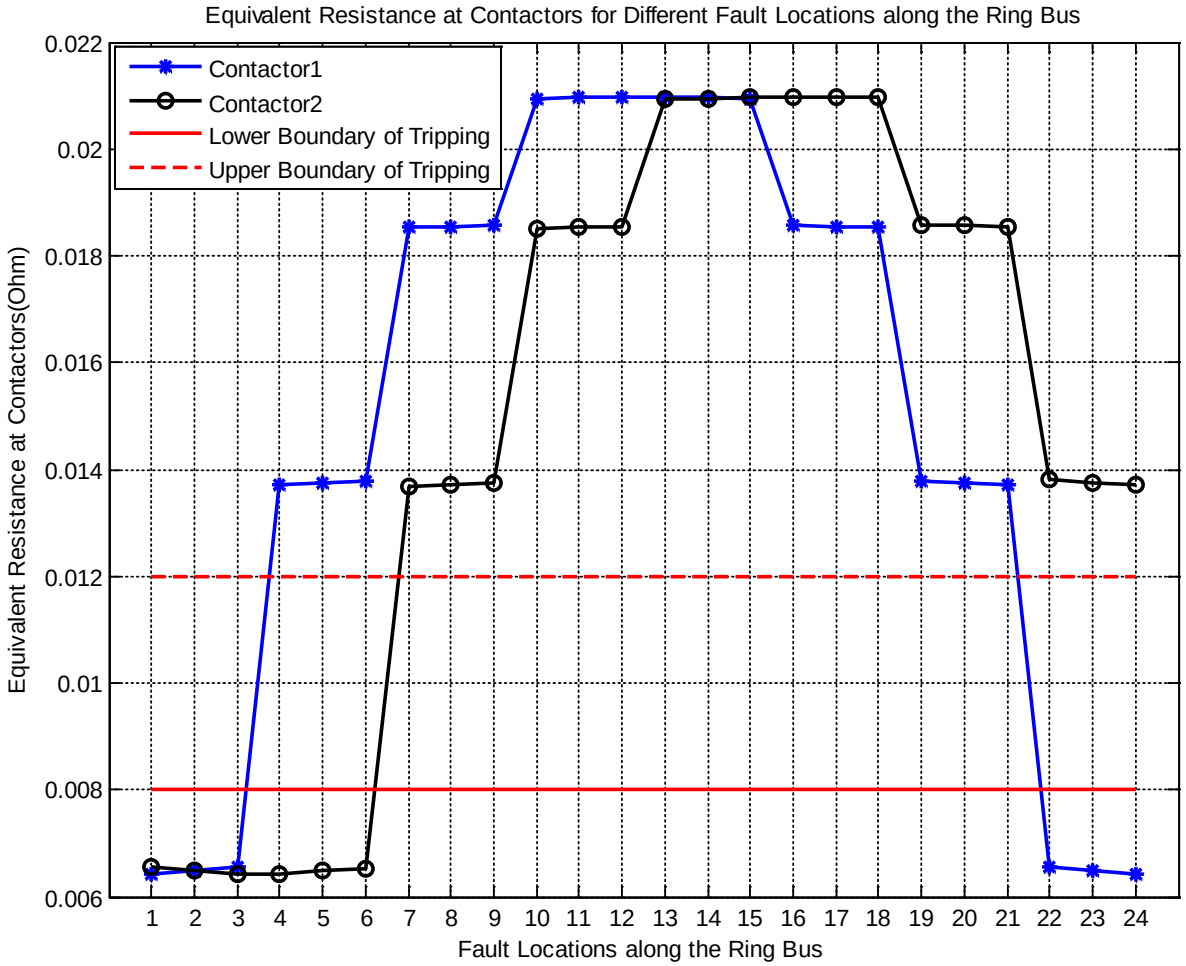


Figure 36 Equivalent resistance at contacor1&2 for different fault locations along the ring bus

7 DISCUSSION, CONCLUSIONS AND RECOMMENDATIONS

Sections 1 and 2 summarized the overall report and introduced this research topic respectively. Device level studies relating to power converters were elaborated upon in section 3 (MMC converter integration) and section 4 (DC-DC converters coordination for fault ride through capability). On the other hand, system and subsystem level analysis was conducted to propose an overall fault management approach. In this regard, the CFM system was explained in section 5 followed by the LFM in section 6 to offer redundancy. This section primarily focuses on planned research in FY 2015 which builds on work detailed in this report. Further, this section also highlights anticipated experimentation using the MVDC testbed at CAPS-FSU.

7.1 Further research into MMC converter studies

A preliminary study of MMC converter and its control has been fulfilled. To build a MMC based MVDC system would be the first practice to study the MVDC system dynamics. Hence, it is logical to design a reduced MVDC benchmark system to get started with. Based on the reduced system the MMC control and the coordination of multi-converter can be well considered and designed for the electric ship application. The subsections to follow elaborate on the issues and proposed solutions regarding current work conducted as well as for near-term plans.

7.1.1 Real-time simulation using FPGA

OPAL-RT, a real-time simulator company enables implementation of the cell model of an MMC in a Field Programmable Gate Array (FPGA). In other words the branch or arm can be simulated using FPGA. The FPGA interfaces the AC model which is implemented as a CPU model. The biggest difference between the FPGA model and the CPU model is that the FPGA model calculates in parallel whereas the CPU model runs in series. The AC system and the converter can be modeled in OPAL-RT CPU, the controller hardware is interfaced with the simulator to receive the current and voltage signals coming from the simulator, and the controller sends the gate drive signals back to simulator. Figure 37 shows a CHIL environment to be implemented in planned further research work.

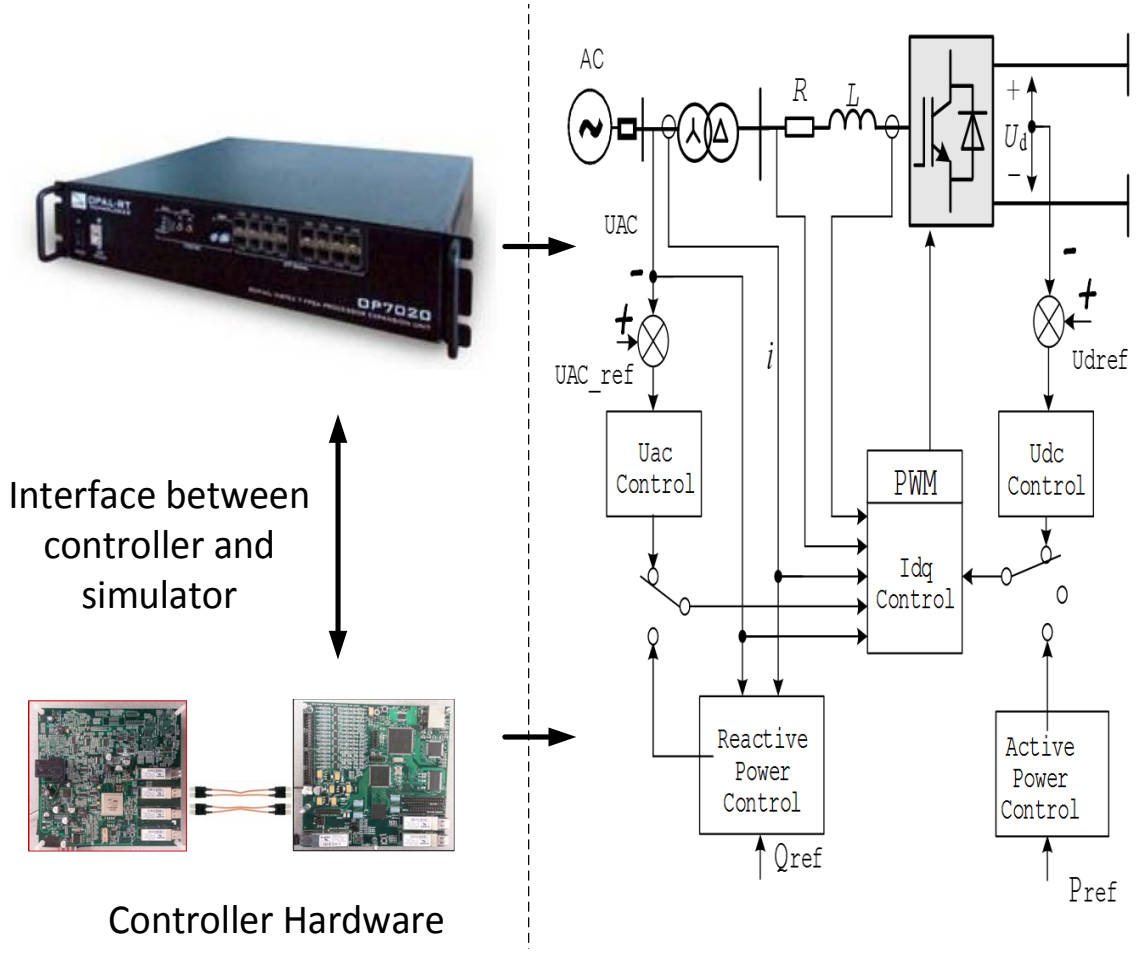


Figure 37 Proposed CHIL setup

An alternative would be to model the entire system in FPGA and connect the controller in the HIL mode. However, challenges related to such implementation need to be studied and consequently addressed.

7.1.2 Interface development for CHIL testing of a full bridge MMC converter

One of the major challenges in MMC-CHIL implementation is handling the input and output signals. The gate pulses are sent from controller to the cells which are modeled in the FPGA or CPU. The cells send back the cell voltage and branch current. The traditional method to achieve this is by using analog channels which involve lots of wiring work. It is practically impossible to implement an MMC-CHIL if there are a large number of cells. Hence, a protocol based optical fiber link is proposed as a viable solution to this problem.

The implementation of full bridge MMC converter and AC system in simulator and the hardware controller are the prerequisites for the CHIL test. After these two steps are done, the next step is to simulate the MMC system to perform a control function similar to that produced in the Simulink environment. The issue is the resulting coordination of the simulator and the controller which is time consuming to debug.

Details of the CHIL setups (CHIL-1 and CHIL-2) at CAPS-FSU have been elaborated upon in section 2.2.3. It is useful to reiterate that the commercially available AC800PEC is used in CHIL-1 as the controller with RTDS being the simulator. The CHIL-2 setup utilizes the USC's universal controller hardware and OPAL-RT which is a different real-time simulation platform to the RTDS (used in CHIL-1). This serves as a basis to compare experimental results from USC as the CHIL-2 setup represents

USC's lower power scale hardware. Another benefit elaborated earlier in section 2.2.3 pertains to the possibility of interfacing firing pulses and other controller signals via fiber optics which is promising from the point of view of reducing analog wiring significantly.

7.1.3 Development and CHIL testing of the fault management scheme

A controllable DC side is the objective of this work. The full bridge cell can not only cut off the fault current which leads to an interrupt of DC power supply, but also perform a fault current limiting function which provides a flexible DC fault defense behavior. To the writer's best knowledge, limiting the DC fault current by MMC converter its self has not been fully studied yet.

Finally, the fault management algorithm in an MVDC shipboard system needs to be tested to verify the fast DC side control strategy. Multi-MMC converters are used in this scenario to provide more flexibility for the system to successfully manage the DC fault within the 8ms goal.

7.2 DC-DC zone converter fault ride through analysis

7.2.1 Issues assessed and addressed

Following are any issues that were addressed or need to be addressed relating to this particular sub-topic within the overall task.

1. **Short circuit fault** – At the occurrence of a short circuit fault on the load side, the output capacitor will generate a large inrush current to feed the fault point. However, to achieve the function of supplying the zonal load, this capacitor cannot be completely removed or reduced in magnitude.
2. **Zonal converter** – The converter that supplies power to a zone needs to switch into a fault control mode after a fault event occurs. The trade-off is between robustness and response time which should be considered carefully in the design of a fault detection logic as well as a mode transfer logic.
3. **Stability during switching** – Switching between normal operation mode and fault protection mode during fault dynamic may cause stability issues.

7.2.2 Conclusions and recommendations

This work within the overall task-4.2.1 proposed a novel control which can allow DAB DC/DC converter to operate at a very wide input voltage range. This control strategy enables the power converter to continue operating at the time a fault occurs on the input side of the DC/DC converter (or the MVDC bus). Also, the output side hold-up capacitor has been analyzed and designed to maintain the voltage of zonal load within an acceptable range during the fault period.

7.2.3 Planned future work

For the near future term, validation of the present work done and further development in the design is a top priority. The primary focus for this sub-task is improving the converter-based fault management solution. The anticipated system design is to achieve the following functions:

1. **Short circuit ability at both input and output –** The present DAB topology and proposed control can achieve wide input voltage change. However, further research is needed to allow short circuit at both input and output of the converter, while maintaining the zone load support function. This aim requires the converter can be controlled as a current source at both input and output port, and still have certain amount of energy storage in the converter. It will be a challenge

for standard DAB converter to meet these requirements, other alternative topologies need to be integrated.

2. **Advanced fault-ride through control –** The control strategy presently needs to switch between the normal and fault operation modes, which can cause transient issues. Advanced fault-ride through control is needed in order to achieve smooth conversion between normal operation and fault operation. It is best to design a control strategy that perform the operation mode conversion seamlessly and without causing any stability issues.

7.3 Further studies necessary for the CFM and LFM approaches

A detailed discussion on the issues, outcomes and future work relating to the CFM approach is contained in section-6 and the associated PhD thesis [13]. This subsection mainly highlights the collaborative studies needed to investigate both CFM and LFM approaches together, thereby addressing and ironing out challenges and issues that may arise.

7.3.1 Issues that need attention

Sections 5 and 6 dealt with the research concerning the LFM and CFM approaches respectively. Detailed in these sections are the necessary analyses and research done to propose means of tackling the overall task.
However, there remain questions to be resolved in order to further validate these approaches. These major issues are,

- **The interaction between CFM and LFM**
  - Interference problems to be studied in greater detail
- **Performance of LFM under varied conditions**
  - Implementation in a multi-terminal close-loop ring bus system
  - Response to different load types other than constant resistive loads
- **Accuracy of fault detection**
  - Robustness of the fault detection algorithm of LFM to withstand severe noise interference
  - Method to reconfigure the equivalent resistance when there is considerable inductance on line
  - Speed and reliability to identify short-circuit fault conditions against normal operation transients
- **MMC converter related experimentation**
  - Speed of interrupting the fault current or to limit the fault current
  - Necessary capacitance on MMC side or load converter side
- **Estimation of energy dumped into the fault during the transient**
  - The characteristic of the DC arc across the contactors and time needed to extinguish the arc

7.3.2 Integration of LFM with CFM

Future work will have to investigate the integration of LFM with CFM that relies on communication for a more accurate localization of faults. The combination of different fault protection scheme can increase the reliability of the system even in the harshest condition. However Interference between the two fault management schemes needs to be studied and avoided.

7.3.3 Implementation of LFM in a baseline model of close loop ring bus system

Future work will need to test the reliability of LFM in a close loop ring bus system based on current development. LFM will be modified to adjust various fault scenarios within close loop ring bus system. This also includes study and verification of LFM for line-to-line fault within bipolar DC bus.

7.3.4 Implementation of LFM under different load types

Current development of LFM assumes all the major loads within the system are constant impedance loads. Thus, the requirements for shut-down of source-side converters and open-operation of designated contactors may be relatively simple because of the vast difference between apparent resistance of the normal working loads and a short circuit. However, there may be constant power loads or other specification of load characteristics in the real application. So far it is not yet confirmed that LFM approach is true for constant power loads, where the load resistance rapidly decreases as system voltage collapses, which make it not obvious when a converter should actually shut off or when a contactor should properly open. Besides, there are other factors need to be considered when applying LFM to different loads. For example, whether these loads are capable of low-voltage cut-off or low-voltage ride-through? The former one will make LFM algorithm easier to locate the fault, while on the contrary the latter one will make the case more difficult. More specifically, if loads are designed with hold-up devices such as input diodes and capacitors, all the loads would stop drawing power from the main bus when voltage collapses, and until the capacitor voltage decreases to the level of the bus voltage. Therefore, it is necessary to figure out how fast does the capacitor voltage decrease to the level of the bus voltage during fault condition, and whether it provides enough time to assess the fault situation and reconfigure. Also, it is important to evaluate the impedance characteristics of those input capacitors during system re-energizing, because they may behave like low impedance when being charged, which may trigger the converters to go into current-limiting mode unexpectedly.

7.3.5 Study of fault detection and coordination solution of LFM under severe noise condition

The ability of noise rejection for fault detection and coordination of LFM has been studied in previous work. However, noise produced by the switching of MMC converters as well as the arcing at fault location need to be further analyzed, due to the fact that they may significantly affect the performance of LFM fault detection and coordination. Meanwhile, a detailed model of arc characteristics at fault needs to be derived.

7.3.6 MVDC hardware validation of LFM

LFM has been verified in both simulations at the medium voltage level and experimentally at the low voltage, low power level. These results provide confidence that LFM can be tested for a higher voltage and power level. Future work will require the hardware validation of this fault protection scheme with appropriate experiments at the medium voltage and megawatt level.

7.4 MVDC fault management PHIL testbed at FSU

The development of a MVDC fault management PHIL testbed at FSU/CAPS is proposed that will use the four, high-power MMC converters in the MVDC test facility to support investigations into the fault management of a representative shipboard, ring-bus topology. The proposed power hardware in loop (PHIL) capability will also provide insight into the overall- fault characteristics and protection system responses of a full-scale, ship power system during parallel operation of multiple PE converters. In each

case, the testbed cable impedances will be scaled representations of anticipated MVDC bus impedances onboard a full-scale ship.

7.4.1 Testbed Topology

The fault management testbed at CAPS will be a PHIL implementation of the power system topology shown in Figure 38. This power system design is a "reduced-capability" version of the full-ship MVDC power system topology illustrated earlier in Figure 1.

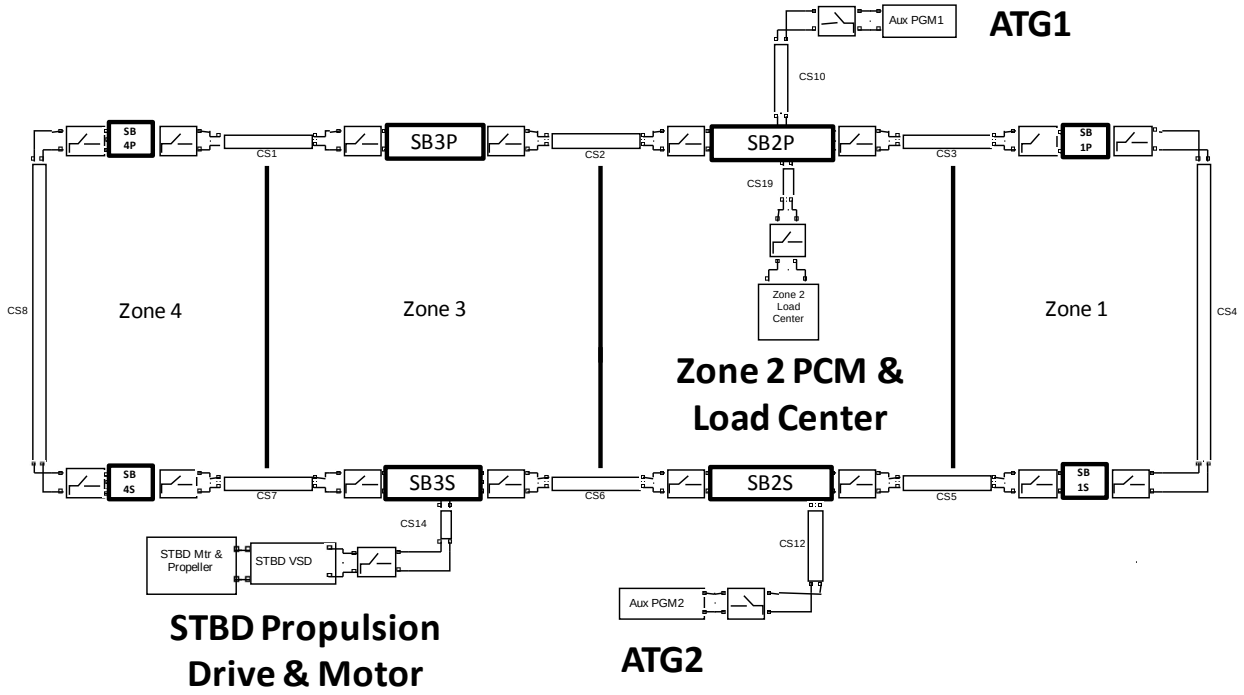


Figure 38 Reduced capability topology of the proposed MVDC fault management PHIL testbed

Implementing the reduced-topology power system at CAPS will require configuring the four MMC converters of the MVDC test facility, the RTDS, the VVS, three MVDC disconnect switches, and a custom, MVDC cable bus circuit according to the scheme laid out in Figure 39. This topology was designed to enable PHIL testing of a ship power system which is capable of:

1. Steady-state operation in split-plant or connected-ring bus configuration,
2. Switching between split-plant- and ring-bus configurations,
3. Representing each of the following ship power system functions:
   a) Power generation (i.e. one 4 MW ATG on each of the longitudinal MVDC buses (i.e. port, and starboard),
   b) Power conversion (i.e. DC/DC converter in Zone 2),
   c) Power distribution (i.e. switchboards and cables),
   d) Electric propulsion (i.e. 4160 V, 36 MW, wire wound AC motor and DC/AC drive converter), and
   e) Mission- and ship service-related electrical loads (i.e. 4 MW total aggregation of Zone 2, Type 1, 450 VAC loads lumped by functional category at the 1 kV LVDC power distribution bus level),
4. Supporting the use of MMC hardware in a PHIL test setup to represent the following:
   a) A complete ATG genset,
   b) The AC/DC converter alone in an ATG,
   c) The DC/AC converter in the propulsion motor drives, and
   d) The DC/DC converter interfaces between the MVDC- and LVDC distribution buses.

The MVDC bus voltage in the PHIL setup is assumed to be 5000 VDC between the positive and negative rails. Three DC disconnect switches are installed in the circuit. D2 and D3 represent the bow and stern cross-hull contactors, respectively. D1 is provided as a means of isolating a high-current, rail-to-rail fault. The next section provides design details- and experimentation plans for the PHIL implementation of these ship power system capabilities.

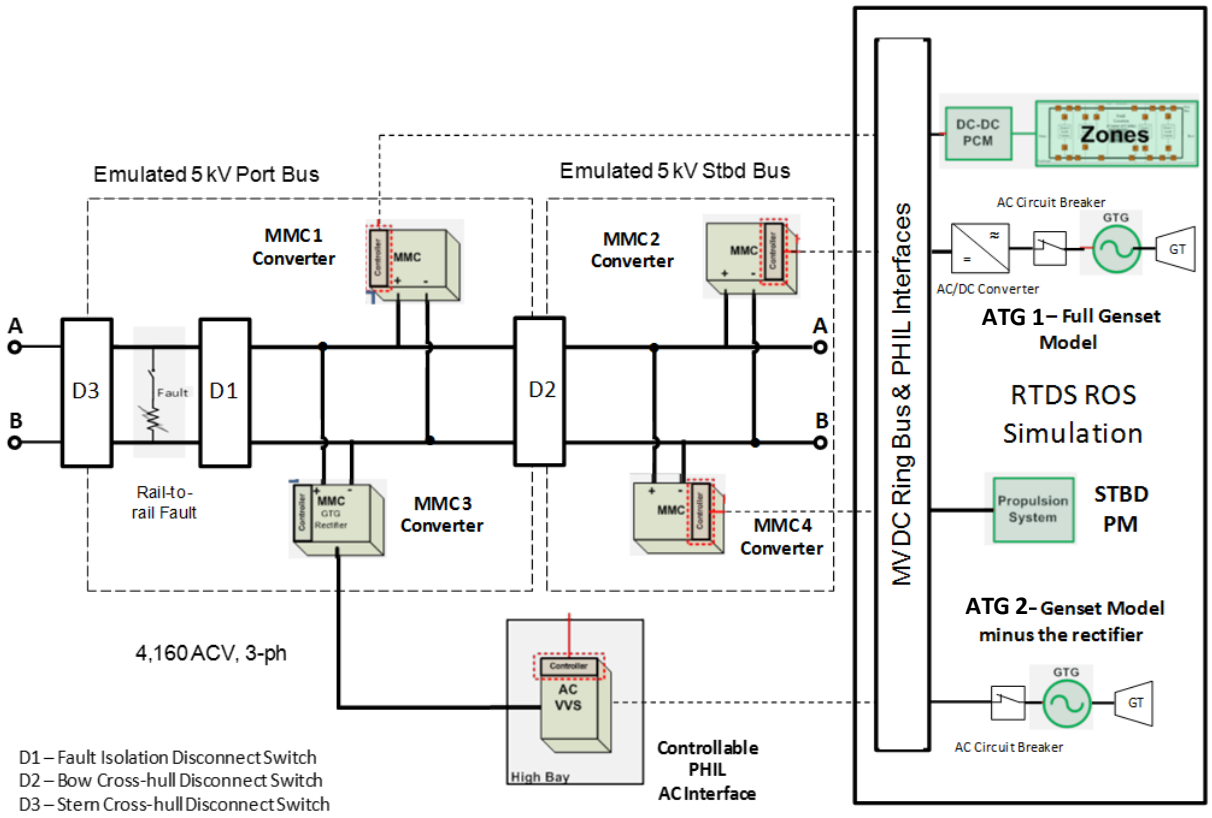


Figure 39 MVDC Fault Management Testbed Topology

7.4.2 PHIL Implementation

It is proposed that three of the four MMC converters in the MVDC test facility be connected to the RTDS ROS via PHIL interfaces, and be controlled so as to represent the following converters in the ROS:

- MMC1 = DC/DC Power Conversion Module in Zone 2
- MMC2 = Full ATG2 genset
- MMC3 = AC/DC rectifier in the ATG1 genset
- MMC4 = DC/AC inverter feeding power to the starboard propulsion motor

Note that whereas MMC2 will be manipulated by the ROS to emulate performance of a full ATG2 genset, MMC3 will only represent the AC/DC converter in ATG1. The variable voltage source (VVS) is used to emulate the prime mover in the genset. This makes it possible to demonstrate the impact of high-current DC bus faults on gas turbine dynamics. The cable segment identifiers in Figure 39 are mapped onto their corresponding testbed cable segments in Figure 40.

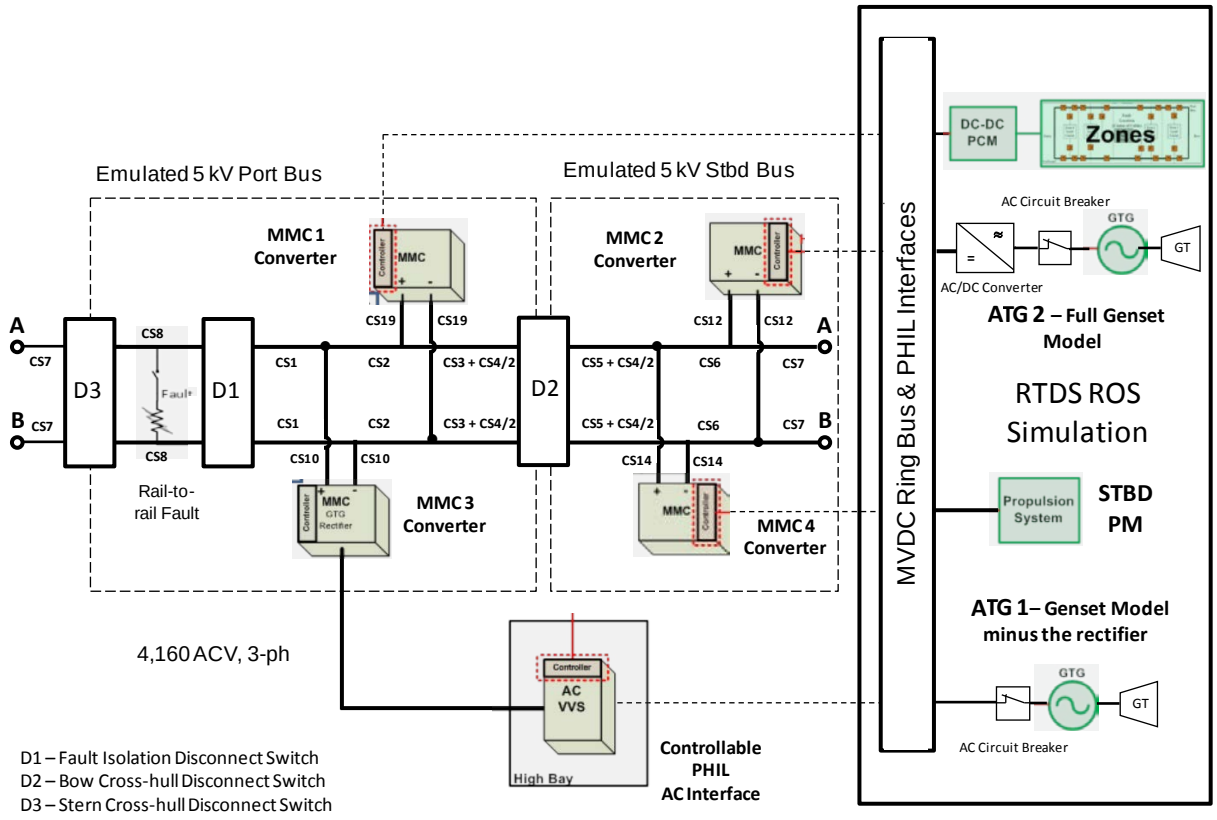


Figure 40 MVDC Ship model-to-testbed cable mapping

7.4.2.1 PHIL Scaling Factors

The system base/rated power for this reduced ship model is 8 MW, i.e. the total installed power level. For the hardware testbed, a base power rating of 1 MW has been chosen. This figure was selected because of the margin it provides to excursions in power level up to the maximum MVDC testbed output power of 1.25 MW. In addition, with a bus voltage of 5 kV, a 1 MW power rating yields a convenient maximum current value of 200 A.

Knowing that the ship model and the hardware testbed have the same rated, bus voltage of 5000 VDC, it is not necessary for the PHIL interface algorithm to scale voltage signals that are passed between the software and hardware sides of the test setup. However, current signals must be scaled using the following scaling factors in order to ensure equivalent, per-unit performance of the two systems:

- Ship model to hardware testbed: Multiply current signal values by 8.
- Hardware testbed to Ship model: Multiply current signal value by 1/8 (i.e. 0.0125).

The cable impedances for the hardware testbed must also be scaled up by an 8-to-1 factor with respect to the cable impedance values employed in the MVDC ship model. The key data for performing this cable scaling process are provided in Table 8. Two types of medium voltage DC cable are represented in the E-ship model. Their technical characteristics are given in a note to the table. The cable types differ only in their specified ampacity, as indicated by a cross-sectional area of 400 mm^2 or 630 mm^2. The values of total resistance, capacitance, and inductance given for the E-ship model cables were calculated from the values for cable length, resistance/inductance per unit length of 400 mm^2/630 mm^2 type cable, and the number of parallel cables in a cable run. Total impedance of the ship model cables was calculated from the figures for total resistance and total inductance.

The total impedance values for the E-ship model were then scaled-up for the PHIL testbed by multiplying the total impedance and total resistance values by the scaling factor of 8.0. Scaled-up cable inductance was calculated from scaled-up impedance and resistance.

The last step in the PHIL testbed cable scaling process is to determine how long the testbed cables need to be in order to provide the amount of scaled-up resistance specified for each cable segment. It is desirable to use the same nomenclature cable in the testbed setup as the E-ship model employs so that the fundamental characteristics of cable construction can be retained. Since the scaled testbed cable segments are now eight times longer than in the ship model, the only practical way to do this is to choose a new MVDC cable for the testbed that is issued by the manufacturer as a member of the same nomenclature family as the ship model cables, but with a cross sectional area (i.e. A) that is one eighth or less of A for the ship model cables. Correspondingly, the resistance per unit length (μΩ/m) of the new cable is increased approximately eight times, which in the end, yields an eight-fold reduction in required cable length for the PHIL test setup.

Table 9 gathers together the pertinent data for exercising this process using the family of single core, medium voltage (3.8/6.6 kV) cables manufactured by the Caledonian company. Values of μΩ/m for the two cable types represented in the E-ship model (i.e. 400mm^2 and 630mm^2) are highlighted. In addition, data is highlighted for a third cable in this family of cables for which the cross sectional area (i.e. 50 mm^2) is one-eighth of the ship model cable with the smallest value of A. Its resistance-per-unit length is 387 μΩ/m, compared to 47.0 μΩ/m and 28.3 μΩ/m for the type 400mm^2 and 630 mm^2 cables respectively. Theoretically, one could chose the smallest cross-sectionalized cable in the family of cables (i.e. 25 mm^2) for use in the testbed in order to keep cable lengths to an absolute minimum. However, the ampacity, or current rating of whatever cable is selected must be greater than the maximum steady-state current level of the MMC converters in CAPS' MVDC test facility. A value of 229 A is assumed for this current limit, which is based on a manufacturer-specified 209 A threshold for the onset of current limiting, plus a 10% margin of excess current-handing capability. Table 8 shows that a 50 mm^2, copper, 3.8/6.6 kV Caledonian cable that is unarmored, and flat-touching through duct work carries a current rating of 220 A. The same cable that is run outside of a duct through the air can safely carry up to 295 A (not shown in table). Therefore, this 50 mm^2, Caledonian cable is recommended for use in the Fault Management PHIL testbed. The required length of this cable for each cable segment in the testbed setup is provided in Table 8.

E-ship model DC cables represented in fault management PHIL testbed					E-ship model cable parameters** total values of resistance (R), capacitance (C), inductance (L) and impedance (Z)				Scaled-up fault management PHIL testbed cable parameters			Cable length exhibiting scaled-up cable resistance#	
Cable ID	**Cable type by cross-sectional area (mm^2)**	**Routing**	**feet**	**meters**	**R (mΩ)**	**C (nF)**	**L (μH)**	**Z (mΩ)**	**R (mΩ)**	**Z (mΩ)**	**L (μH)**	**feet**	**meters**
CS1	630	Zone 3 to Zone 4 Port Ring bus	136	41.5	0.59	60.2	9.534	3.64	4.7	29.1	76.3	39.8	12.1
CS2	630	Zone 2 to Zone 3 Port Ring bus	97	29.6	0.42	42.9	6.8	2.6	3.3	20.8	54.4	28.4	8.6
CS3	630	Zone 1 to Zone 2 Port Ring bus	94	28.7	0.41	41.6	6.59	2.52	3.2	20.1	52.7	27.5	8.4
CS4	630	Bow Cross-hull Link	97	29.7	0.42	42.9	6.8	2.6	3.3	20.8	54.4	28.4	8.6
CS5	630	Zone 1 to Zone 2 Stbd Ring bus	80	24.3	0.35	35.4	5.608	2.14	2.8	17.1	44.9	23.4	7.1
CS6	630	Zone 2 to Zone 3 Stbd Ring bus	97	29.6	0.42	42.9	6.8	2.6	3.3	20.8	54.4	28.4	8.6
CS7	630	Zone 3 to Zone 4 Stbd Ring bus	90	27.4	0.39	39.8	6.309	2.41	3.1	19.3	50.5	26.3	8
CS8	630	Stern Cross-hull Link	137	41.8	0.59	60.6	9.604	3.67	4.7	29.3	76.8	40.1	12.2
CS10	400	ATG1 to MVDC bus	73.5	22.4	0.53	28.1	5.377	2.09	4.2	16.8	43	35.7	10.9
CS12	400	ATG2 to MVDC bus	87	26.5	0.62	33.3	6.364	2.48	5	19.8	50.9	42.3	12.9
CS14	630	STBD PM to MVDC bus	95.5	29.1	0.36	19.1	3.658	1.42	2.9	11.4	29.3	24.3	7.4
CS19*	400	Zone 2 PCM to MVDC bus	50	15.2	0.59	60.2	9.534	3.64	4.7	29.1	76.3	39.8	12.1

Cable Manufacturer: Caledonian (online reference – http://www.caledonian-cables.co.uk/DdFls/MV/Medium%20Voltage%20Cables.pdf)
Nomenclature: Medium voltage cables to BS 6622/BS 7835, Rated voltage: 3.8/6.6 kV
Construction and layout: Single core, copper, unarmored, flat-touching, in duct enclosure

*Assumed same cable length as for CS16.

**Assumed cable manufacturer, nomenclature, and technical characteristics for MVDC ship model:

Cable Type ID: 400 mm2 (nominal cross-sectional area)
DC resistance per unit length: 28.3μΩ/m
Capacitance per unit length: 726 pF/m
Inductance per unit length: 460 nH/m

Cable Type ID: 630 mm2 (nominal cross-sectional area)
DC resistance per unit length: 47.0μΩ/m
Capacitance per unit length: 627 pF/m
Inductance per unit length: 480 nH/m

#Assumed cable manufacturer, nomenclature, and technical characteristics for Fault Management PHIL Testbed:
Cable Type ID: 50 mm2 (nominal cross-sectional area)
DC resistance per unit length: 387μΩ/m
Capacitance per unit length: 321 pF/m

Table 8 Fault management PHIL testbed cable parameters

Nom. Cross-section Area (mm^2)	Current Rating (A)	DC Resistance per Unit Length (μΩ/m)
25	165	727
35	185	524
50	220	387
70	270	268
95	325	193
120	370	153
150	415	124
185	465	99.1
240	540	75.4
300	610	60.1
400	690	47.0
500	790	36.6
630	890	28.3

Table 9 Cable data for selection of PHIL testbed cable

7.4.3 Proposed Action Plan

It is proposed that the following plan of action be followed in developing the MVDC fault management PHIL testbed at CAPS:

1. Develop the reduced topology ship model of Figure 38 in Simulink and PLECS, using average-value converter models to the extent possible.
2. Develop a CHIL-version of the reduced topology ship model on the RTDS using switching models to help validate the reduced topology ship model, and to use as the ROS during PHIL testing as well as the actual, future PHIL test setup.
3. Finally, build the PHIL test setup and used to demonstrate MMC fault management solutions in hardware.

7.4.4 Power converter models

A related interest regarding future planned experiments is the integration of converter models within the test setup. At this stage, details have been explained regarding MMC converter modeling and downstream DC-DC converter coordination and control studies. Further analysis is necessary to enable integration of converter models into the MVDC testbed for the specific purpose of fault current limiting. Development of an average value model is on-going at CAPS, brief details of which are displayed through MATLAB code in Appendix-B.

8 REFERENCES

[1] Winkelnkemper, M.; Korn, A.; Steimer, P., "A modular direct converter for transformerless rail interties," *Industrial Electronics (ISIE), 2010 IEEE International Symposium on* , vol., no., pp.562,567, 4-7 July 2010

[2] Myungchin Kim; Kwasinski, A., "Decentralized Hierarchical Control of Active Power Distribution Nodes," *Energy Conversion, IEEE Transactions on* , vol.29, no.4, pp.934,943, Dec. 2014

[3] Cairoli, P.; Kondratiev, I.; Dougal, R. A., "Coordinated Control of the Bus Tie Switches and Power Supply Converters for Fault Protection in DC Microgrids," *Power Electronics, IEEE Transactions on* , vol.28, no.4, pp.2037,2047, April 2013

[4] Cairoli, P.; Dougal, R.A.; Ghisla, U.; Kondratiev, I., "Power sequencing approach to fault isolation in DC systems: Influence of system parameters," *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE* , vol., no., pp.72,78, 12-16 Sept. 2010

[5] Cairoli, P.; Dougal, R.A.; Lentijo, K., "Coordination between supply power converters and contactors for fault protection in multi-terminal MVDC distribution systems," *Electric Ship Technologies Symposium (ESTS), 2013 IEEE* , vol., no., pp.493,499, 22-24 April 2013

[6] Cairoli, P.; Dougal, R.A., "Using apparent resistance for fault discrimination in multi-terminal DC systems," *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE* , vol., no., pp.80,87, 15-19 Sept. 2013

[7] Cairoli, P., Ghisla, U., Dougal, R., Ginn, H., Liu, X., Yu, M., Steurer, M., "Fault Current Limiting Methods", Technical report submitted to the ONR, October 2013.

[8] Jih-Sheng Lai; Fang Zheng Peng, "Multilevel converters-a new breed of power converters," *Industry Applications, IEEE Transactions on* , vol.32, no.3, pp.509,517, May/Jun 1996

[9] Fang Luo; Jian Chen; Xinchun Lin; Yong Kang; Shanxu Duan, "A novel solid state fault current limiter for DC power distribution network," *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE* , vol., no., pp.1284,1289, 24-28 Feb. 2008

[10] Baragona, T.A.; Jordan, P.E.; Shiffler, B.A.; "A Breaker-Less, Medium Voltage DC Architecture," Newport News Shipbuilding Division of Huntington Ingalls Industries

[11] Tucker, J.; Martin, D.; Mersenski, R.; Barkley, A.; Cairoli, P.; Ghisla, U.; Riccobono, A.; Dougal, R.; Santi, E., "Fault protection and ride-through scheme for MVDC power distribution systems utilizing a supervisory controller," Electric Ship Technologies Symposium (ESTS), 2011 IEEE , vol., no., pp.319,325, 10-13 April 2011

[12] Hagiwara, M.; Maeda, R.; Akagi, H., "Negative-Sequence Reactive-Power Control by a PWM STATCOM Based on a Modular Multilevel Cascade Converter (MMCC-SDBC)," *Industry Applications, IEEE Transactions on* , vol.48, no.2, pp.720,729, March-April 2012

[13] Haimin Tao; Kotsopoulos, A; Duarte, J.L.; Hendrix, M.AM., "Transformer-Coupled Multiport ZVS Bidirectional DC–DC Converter With Wide Input Range," Power Electronics, IEEE Transactions on , vol.23,no.2,pp.771,781,March2008

[14] Liu, X., Ph.D. Thesis. "A Centralized Fault Management Approach for Smart Grid Protection," Center for Advanced Power Systems, Florida State University, 2014.

9 APPENDIX-A

It is relatively easier to evaluate the parameters of the MMC converter system and the controller performance in using p.u. values as compared to the SI system, especially when the transformer is introduced in the system. For instance, a 5 kVAr reactive power oscillation brought about by controller is acceptable when the system capacity is 5000 kVA (0.1% = 5 kVAr), however, it seems too much if it happens in a smaller or weak source system. Hence, if a per-unit system is introduced, it becomes easier for engineers to evaluate the system performance and they will be able to tune the controller easily. Another reason to apply p.u. system is that it is less risky to have a software crash in DSP (digital signal processor) since it is less likely to have trouble with the calculation overflow. A p.u. system utilized in VSC-HVDC with MMC topology can be applied here. The bases in AC system and DC system are given as:

$$S_{ac,base} = S_N$$
$$U_{ac,base} = \sqrt{2}U_N$$
$$I_{ac,base} = 2S_{ac,base}/3U_{ac,base}$$
$$Z_{ac,base} = U_{ac,base}/I_{ac,base}$$

Where;
S_N = nominal system capacity in KVA
U_N = nominal AC phase-to-ground voltage (RMS)
$U_{ac,base}$ = peak AC phase-to-ground voltage
$I_{ac,base}$ = peak phase-to-phase current respectively

For the DC side, the equivalent terms are,

$$S_{dc,base} = S_N$$
$$U_{dc,base} = U_{dcN}$$
$$I_{dc,base} = S_{dc,base}/U_{dcN}$$
$$U_{sm,base} = U_{dcN}/\mathrm{N}$$

Where;
$U_{dc,base}$ = DC nominal voltage
$I_{dc,base}$ = DC nominal current (basic frequency components).

In order to develop a controller for MMC system, it is important to transform the system from SI system to p.u. system. One reason is it is easy to evaluate the controller performance in p.u. system, since the data is scaled between (0, 1), and the other reason is the controller can be migrated to another MMC converter system with minor modification. Table 10 shows parameters utilized in MMC Simulink model.

Parameter symbol and formula	Value
$S_{ac,base} = S_N$	$80\ KVA$
$U_{ac,base} = \sqrt{2}U_N = \frac{208}{1.732} \times 1.414$	$169.8\ V$
$I_{ac,base} = \frac{2S_{ac,base}}{3U_{ac,base}} = 2 \times 80 \times \frac{1000}{3 \times 169.8}$	$314.095\ A$
$S_{dc,base} = S_N$	$80\ KVA$
$I_{dc,base} = \frac{S_{dc,base}}{U_{dcN}} = 80 \times \frac{1000}{800}$	$100\ A$
$U_{dc,base}$	$800\ V$
$U_{sm,base} = \frac{800\ V}{N} = \frac{800\ V}{6}$	$133.33\ V$

Table 10 Parameters used for the MMC Simulink model

10 APPENDIX-B

The following model is an average value model of an MMC developed using MATLAB-2013a and PLECs version 3.5. The user edits the m-file run one of eight test cases to execute the following modes with its subcategories:

1. Voltage source mode
    a. Step-up
    b. Step-down
2. Current source FF disabled mode
    a. Step-up
    b. Step-down
3. Current source FF enabled mode
    a. Step-up
    b. Step-down
4. Resistive DC Load step
    a. Step up/down in Voltage Source Mode
    b. Step up/down in Current Source Mode

MMC: Parameters

```
MRUPb = 1.25e6; % Base active power (W)
MRUVrn = 1.0; % Normalized secondary reference voltage
MRUVbd = 6.0e3; % DC voltage base value
MRUIbd = MRUPb/MRUVbd; % DC current base value
MR2Rb = MRUVbd^2/MRUPb; % Resistance base value based on 6kVdc and 1.25 kW

Cr = 2.3e-3; % Capacitor value of each cell
N = 6; % Number of switching modules per arm
MR2Ce = 6*Cr/N; % DC side capacitor value (equivalent capacitance)

k = 0.68; % Inductor coupling factor
L = 2.0e-3; % Branch inductance
Larm = [L/(2*(1+k)) -L*k/(2*(1+k)); -L*k/(2*(1+k)) L/(2*(1+k))];

MRUVba = 3.3e3*sqrt(2/3); % AC side base voltage magnitude
MRUIba = 2*(1.25e6/3)/MRUVba; % AC side base current magnitude
MRUQ = 0.0; % Reactive power control reference power (VARs)
MR1Le = 2.0e-3;     % Equivalent inductance

%% 3-phase voltage source used for testing purposes only
Vmag = MRUVba; % Voltage magnitude (V)
Freq = 2*pi*60; % Frequency (rad/s)
Phi = pi/2;
Van_ph = 0+Phi; % Van Phase (rad)
Vbn_ph = -2*pi/3+Phi; % Van Phase (rad)
Vcn_ph = 2*pi/3+Phi; % Van Phase (rad)

%% Controller setup
% PI-controls

% Outer loops
% Cap V
MR2Kpdc = 9.5;
MR2Kidc = MR2Kpdc*60;
% Reactive power Q
MR2Kps = 0.4;
MR2Kis = 200;
```

```
% Inner loop
% Id
MR2Kpd = 0.08;
MR2Kid = 0.8;
% Iq
MR2Kpq = MR2Kpd;
MR2Kiq = MR2Kid;

% DC loop
% Vdc
MRCKpV = 0.5;
MRCKiV = 125;
% Idc
MRCKpIdc = 10.0;
MRCKiIdc = 1.0;

MRUFf = 400;        % Frequency of DC controls output filter
MRUTf = 1/MRUFf;    % Time constant of DC controls output filter
```

The MMC average value model is embedded into the following system:

1. AC-voltage source with impedance, and
2. Resistive load on DC-side.

MMC Average value model, simulation environment setup and case selection

```
clear;clc;
%% Simulation (Simulink) and base case setup
Ts = 2*25e-6;       % Simulation time-step (s)
TsampF = Ts;
T_sim = 600e-3;     % Simulation time (s)
slxname = 'MMC_AVM'; % Simulink/PLECS model name (*.slx)
Param_MMC_AVM;      % MMC parameters

%% Select mode of operation
% Options
MRUmode_VSM = 0; % voltage source mode
MRUmode_CSM = 1; % current source mode
% Selection
MRUmode = MRUmode_VSM; % VSM by default
MRURFFen = 0;   % 0 - FF disabled, 1 - FF enabled
MRURFF = 28;    % FF term - DC Load impedance (ohm)
%% Voltage or Current requests (scenario setups)
MRUIr_T = [0 T_sim];
MRUIr_A = [0 0];
MRUVr_T = [0 T_sim];
MRUVr_V = [0 0];
if (MRUmode == MRUmode_VSM) % If in VSM, set voltage references. Current references disabled
   MRUVr_T = [0 0.40 0.401 T_sim];
   MRUVr_V = [0 0 5000 5000];
elseif (MRUmode == MRUmode_CSM) % If in CSM, set current references. Voltage references disabled
   MRUIr_T = [0 0.4 0.401 T_sim];
   MRUIr_A = [0 0 200 200];
else % disable both. Not active
   MMC = 'defaulted to VSM mode'
end

% Set load condition
RLoad_T = [0 0.4 0.401 T_sim];  % load resistance step times
RLoad_V = [28.8 28.8 28.8 28.8];% load resistance (28.8 ohm - base)
%% Execute Simulation
tic()
sim(slxname);
toc()
```

This model is equipped with feed-forward term capabilities in current source mode for faster response of current steps. The model is also capable of limiting the current on the DC side to a value of 10% over the rated value thereby preventing extremely high currents in the DC side. However, a more rigorous verification and validation is needed before attempting to use these models for the fault limiting experiments on the MVDC testbed.