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DEVELOPMENT AND TESTING OF A 1 KV SOLID STATE CIRCUIT BREAKER

Technical Report

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Bradley Shonka, Qichen Yang

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1 ACKNOWLEDGEMENTS

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2 EXECUTIVE SUMMARY

Recent increases in dc power system usage have created a need for dc capable circuit breakers. One method to achieve this is through the development of solid state circuit breakers (SSCB) that utilize power electronics to break the circuit. The use of power electronics allows for the breaking of a circuit quickly with no need for a natural current zero-crossing point for arc-less interruption of current. This report details the development of a 1 kV 0.2 kA SSCB. The control scheme is discussed as well as its implementation in real-time simulation (RTS).

3 INTRODUCTION

Recent research and developments in dc power systems has increased the need for reliable methods to break dc current in the case of a current surge. One such method is the use of Solid State Circuit Breakers (SSCB) that utilize power electronics. The use of power electronics to break the circuit allows for faster breaker operation as well as eliminating the need for a natural zero-crossing in the current to achieve an arc-less current interruption. This paper describes the design and operation of a SSCB rated 1.0 kV and 0.2 kA and designed to interrupt a dc circuit with a minimum inductance of $50\,\mu\mathrm{H}$. The primary purpose of these SSCBs is to facilitate benchtop experiments pertaining to dc fault management. The secondary purpose is to use them in combination with a resistive load to simulate pulse loads with high turn-on and turn-off transients.

3.1 Solid State Circuit Breaker

The developed SSCBs, topology shown in Figure 1, consist of two high power Insulated Gate Bipolar Transitors (IGBT) to perform switching operations when the gate drivers are signaled by the controller, and Metal Oxide Varistors (MOV) to clamp the transient voltages following the switch operation. The auxiliary circuit displayed in Figure 2 is used to power the gate driver boards. The IGBTs are mounted on a heat sink that is kept cool using fans that are powered by the circuit depicted in Figure 3. Figures 4-6 display the constructed SSCB and highlight the placement of the main components of the device. The constructed SSCB is composed of the IGBTs mounted on a heatsink. The gate driver boards are mounted atop the IGBTs and the MOVs are suspended above the IGBTs. When the SSCB is in the closed state, the IGBTs remain continuously in the conducting state, and the IGBTs are only switched in order to open the SSCB.

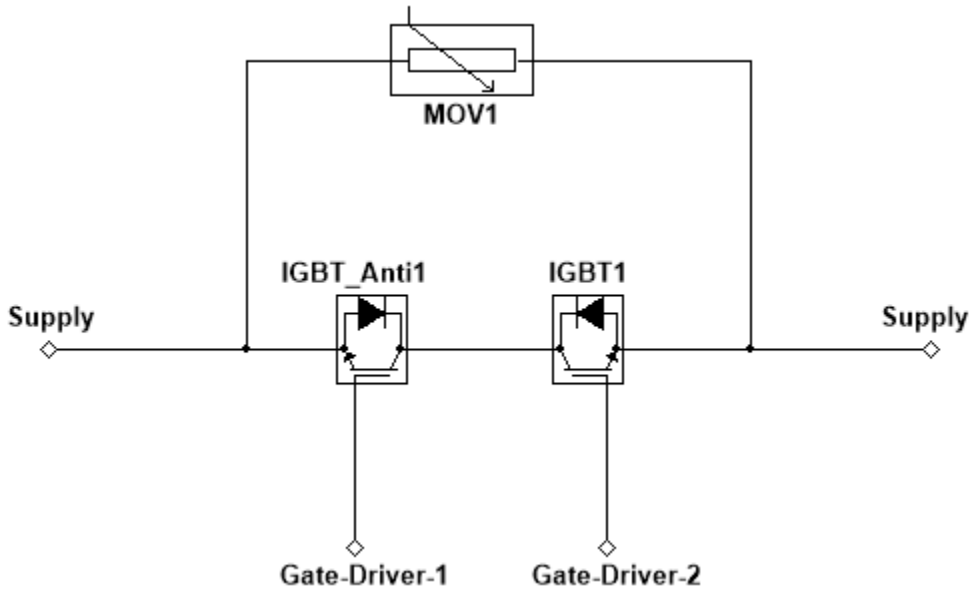

Fig. 1: SSCB Model

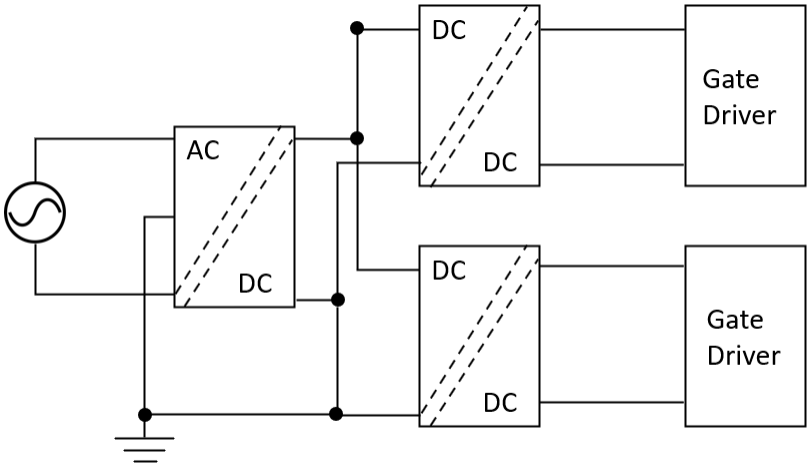

Fig. 2: Gate Driver Auxiliary Circuit

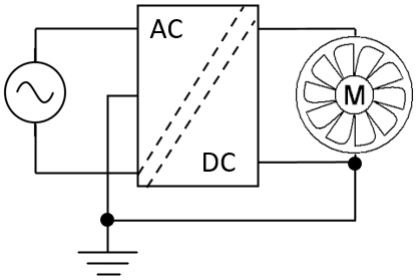

Fig. 3: Heat Sink Fans Auxiliary Circuit

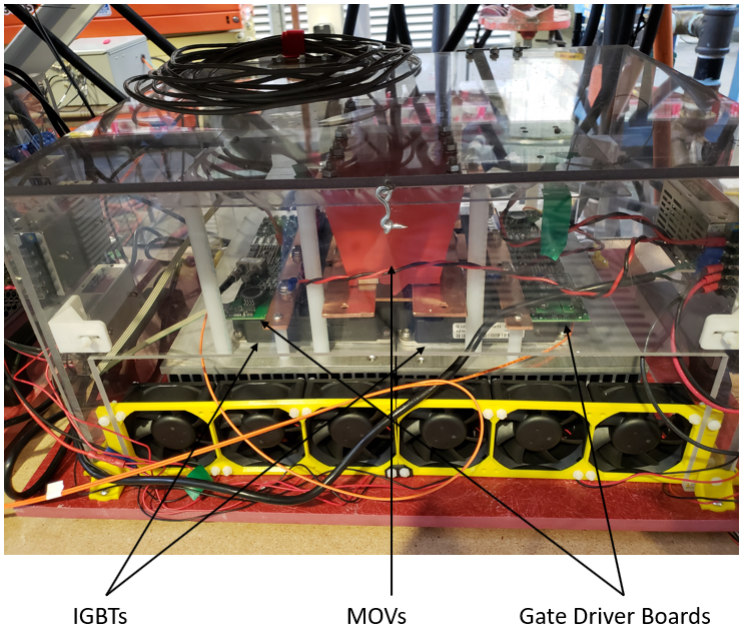

Fig. 4: SSCB Front View

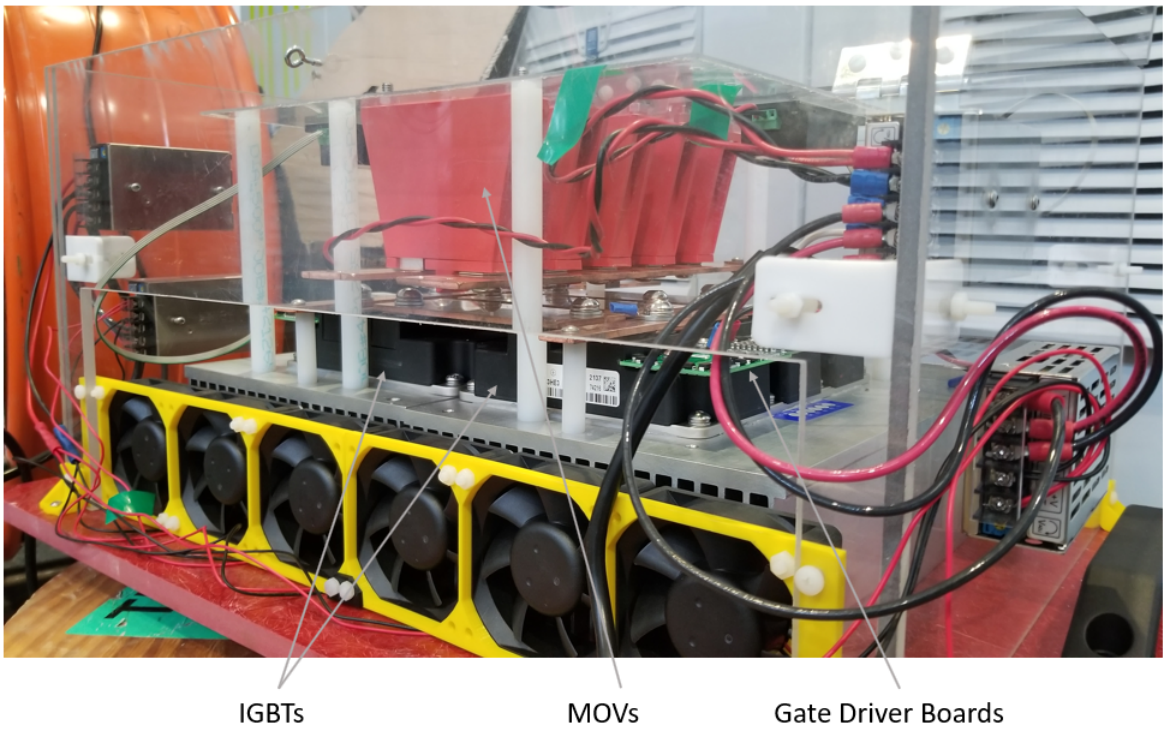

Fig. 5: SSCB Corner View

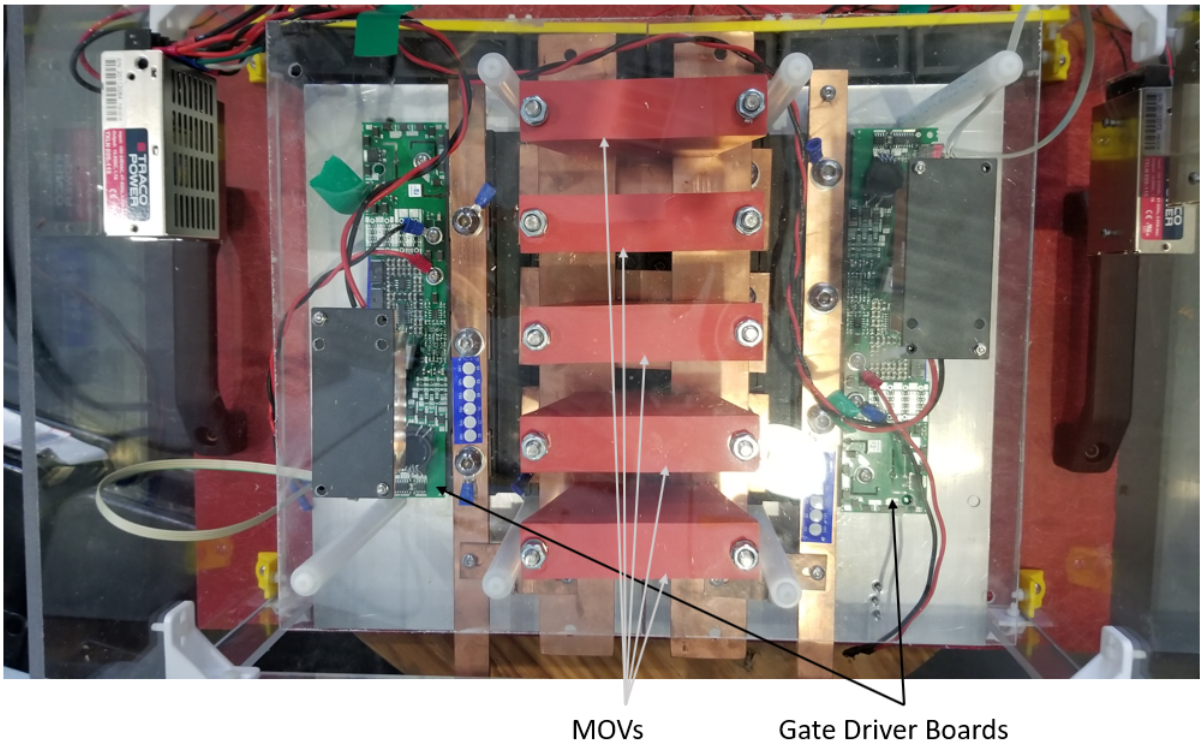

Fig. 6: SSCB Top View

4 CONTROLLER DETAILS

The controller was designed to utilize the input current measurement to determine if an overcurrent event has occurred or if the I2T protection limit has been exceeded. I2T protection is a long-term protection scheme that typically protects the breaker from exceeding thermal limits, but is included in the SSCB's protection scheme to be consistent with traditional breakers and simplify coordination of the protection system. The operator controls were designed to be used to reset the breaker or force a trip or re-closure.

The controller logic, seen in Figure 7, is designed to receive a measurement of the current through the SSCB as well as control signals from the operator. The current measurement is communicated to the time over current (TOC) logic and used to determine if a trip is necessary. The output of the TOC logic is used in a set-reset (SR) latch to lock the breaker in a closed state when a trip is necessary. In order to re-close the breaker it must first be reset using the S_{reset} signal. The output of the SR latch indicates the direction of current flow in which the over-current was detected. The signals S_{trip}, S_{open}, and S_{close} are used to manually open and close the breaker.

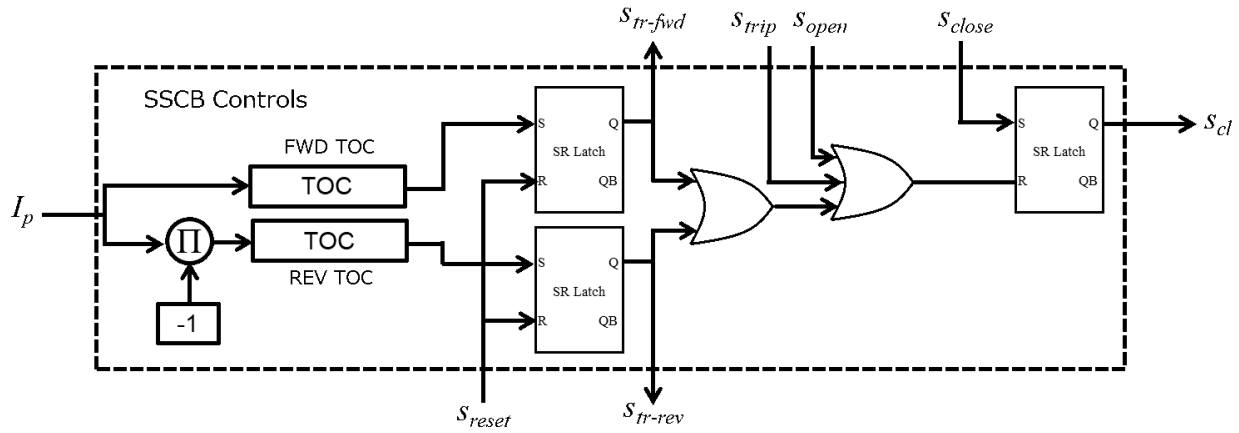

Fig. 7: SSCB Control Logic

Demonstrated by the logic circuit in Figure 8, the current measurement is first divided by the rated current and is compared to pickup threshold multipliers. If the per unit value exceeds either pickup threshold multiplier then a pickup timer is started. The pickup timer is compared to the time delay for each respective trip threshold and a trip is indicated if these delays are exceeded. In parallel the current measurement is integrated and compared to the I2T protection. The I2T protection functions by integrating the measured current and comparing it to the value of the short term pickup threshold squared times the short term delay as seen in equation 1. The integration continues unless the short time pickup threshold is exceeded or the measured current falls below the rated current of the SSCB. The threshold and delay terms are explained in Table 1.

$$I2T = I^2 * N_{st} \tag{1}$$

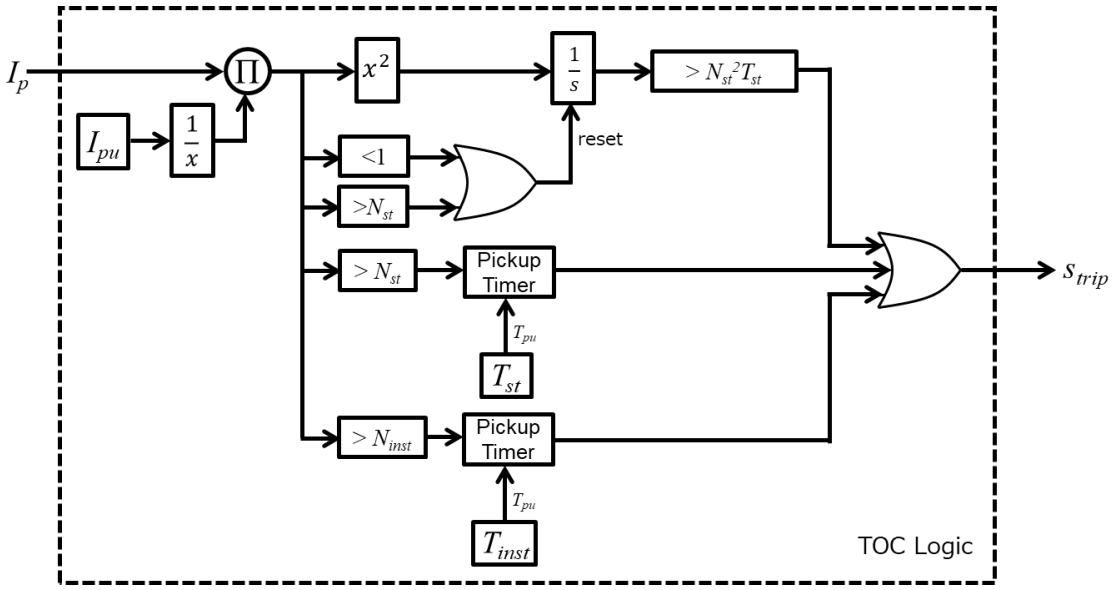

Fig. 8: Time Over Current Logic

Table 1: Circuit Breaker Control Parameters

Parameter	Definition
I_{pu}	Rated Current
N_{st}	Short-term pickup threshold
T_{st}	Short-term pickup delay
N_{inst}	Instantaneous pickup threshold
T_{inst}	Instantaneous pickup delay

4.1 FPGA Controller

A field programmable gate array (FPGA) controller approach was considered in order to reduce the controller latency to 200 ns. The expected reduction in the controller reaction time would provide an opportunity to significantly reduce the minimum required inductance. However, there were difficulties finding an analog-to-digital converter (ADC) that was capable of converting a dc signal at the speed necessary to achieve the desired controller latency. Therefore, the FPGA-based controller is still in development.

4.2 Microcontroller

A microcontroller-based implementation was initially considered for the near-term controller solution, with the intent to achieve a controller latency of not more than $2\,\mu$s. However, some difficulties were encountered with the implementation of this controller. An interface board was needed to pro-

vide the optical signals to the gate-driver boards and to condition current measurements from the SSCB current sensors. The timely implementation of this interface board was hampered by component supply issues and other considerations. Additionally, initial implementations of the control code using floating point operations did not achieve the desired update rate for the controller[1]. Due to schedule considerations, the effort required to reduce the update rate of the controller, and the challenges in the development of the interface board, an alternative approach for rapid prototyping of the controller was used, as discussed below.

4.3 RTS Implementation

In order to expedite the implementation of the controller and to facilitate rapid prototyping and refinement of the control logic, a real-time simulator (RTS) was used to initially serve as the controller for the SSCBs. The control logic for three SSCBs was implemented in the sub-step environment of a NovaCore rack of a commercial RTS developed by RTDS Technologies, operating in real-time with a time-step size of $2.5\,\mu s$. A GTAI card was used for sampling the current measurements from the SSCB current sensors, and a GTDO card, in conjunction with simple fiber transmitter circuits, was used to send the fiber signals to the gate driver boards of the SSCB. This provided for timely execution of the controls, along with the needed peripheral I/O, and provided a flexible platform for rapidly changing the control logic and structure if needed. However, this solution requires the use of a RTS to use the SSCBs, and, therefore, is viewed as a temporary solution for the control platform.

5 MEASUREMENT RESULTS

The test circuit, illustrated in Figure 9, consisted of a 1 kV source, a $60\,\mu F$ capacitor bank, a $60\,\mu H$ air core inductor to limit the di/dt, a 0.014 Ω current-limiting resistor (which was configured for higher resistance values in commissioning tests), and diodes to block ringing in the circuit in the event that the SSCB did not open. While S1 is closed and S2 is open, the voltage source is used to charge the capacitor bank with the SSCB in the open state. Once the capacitor bank is charged, S1 is opened and the SSCB is closed to cause an overcurrent event requiring an instantaneous trip, at 0.525 kA. Current measurements from the SSCB are communicated to the controller. The controller indicates a trip to the anti-series IGBTs that break the circuit. In Figure 10 the test set up is displayed. After a test is completed, S2 is closed to ensure that the capacitor is fully discharged before approaching the test setup.

[1]The microcontroller implementation may be able to achieve improved performance by using integer formulation of the code

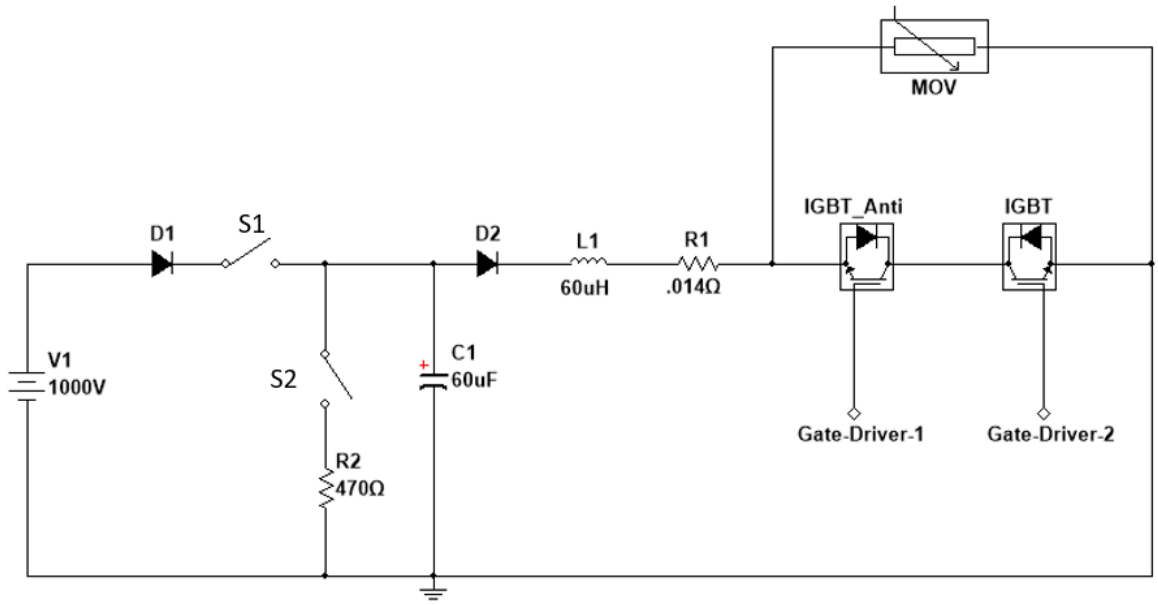

Fig. 9: Measurement Circuit

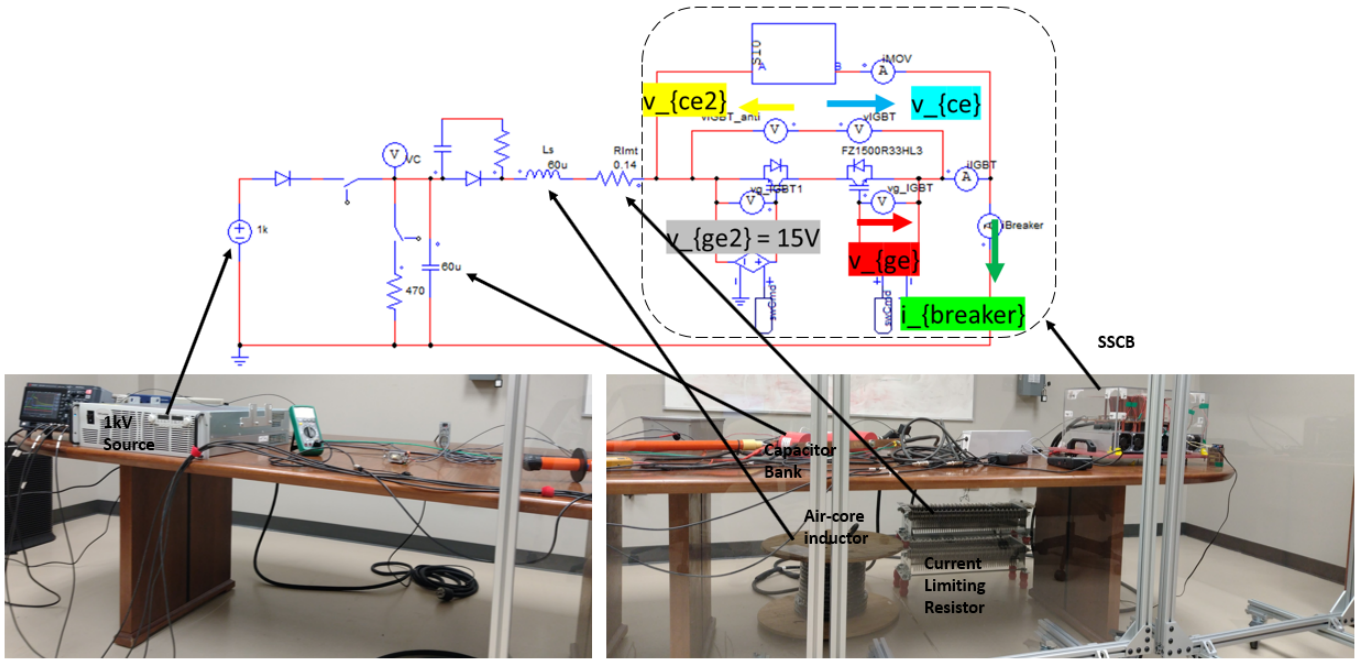

Fig. 10: Test Circuit Physical Components

Theoretical conduction power losses of the IGBTs at rated current can be calculated using equation 2 and equation 3 to calculate the power dissipated by the IGBT and freewheeling diode respectively. The voltage drop across the components is derived from the characteristic values seen in Figure 11 and Figure 12. The on-state resistances are calculated using equation 4 which is the inverse linearized slope of the output characteristics.

The actual conduction losses are calculated using the rated current and the measured voltage drop over the IGBT and the freewheeling diode shown in Table 2. The conduction loss of the IGBT is 276 W and the loss of the diode is 264 W.

$$P_{cond(IGBT)} = V_{CE0} * I + R_0 * I^2 = 1.25V * 200A + 0.00083\Omega * (200A)^2 = 283.2W \quad (2)$$

$$P_{cond(Diode)} = V_{D0} * I + R_{D0} * I^2 = 1.25V * 200A + 0.0008\Omega * (200A)^2 = 282W \quad (3)$$

$$R_0 = \frac{V_2 - V_1}{I_2 - I_1} \quad (4)$$

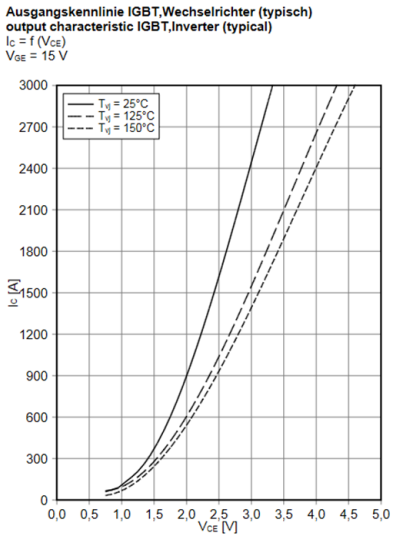

Fig. 11: IGBT Output Characteristics

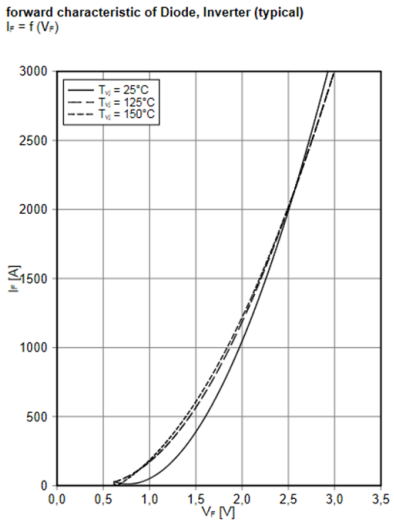

Fig. 12: Forward Characteristics of Anti-Parallel Diode

Table 2: Steady State Voltage Drop at Rated Current

Current (A)	$\mathbf{V}_{CEsat}(V)$	$\mathbf{V}_{fdiode}(V)$
200	1.38	1.32

Figure 13 shows the measurement of the current through the SSCB and the trip indicating signal from the controller. There is a delay between the trip signal and the time that the current peaks and begins to decrease. The peak value of current is reached at $58.78\,\mu s$ and the trip signal is sent at $52.59\,\mu s$. The delay from trip signaled to negative di/dt amounts to $6.19\,\mu s$ delay. Similar results from testing each of the five SSCBs developed are presented in Appendix A.

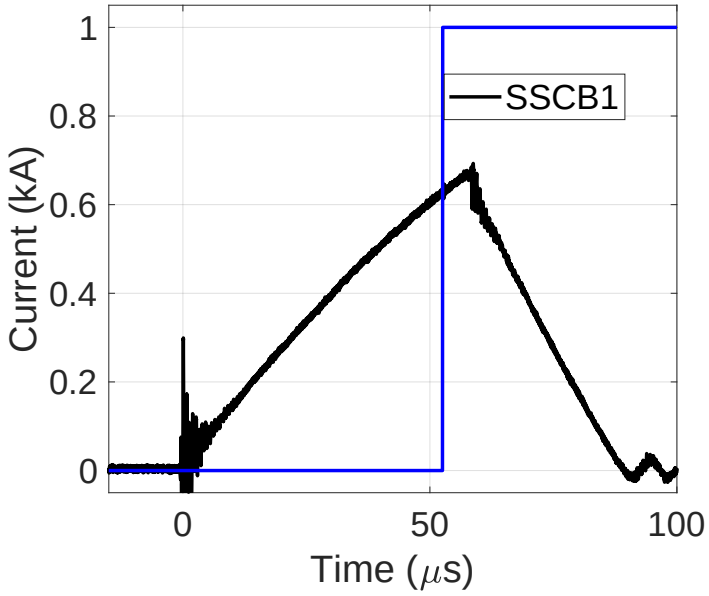

Fig. 13: SSCB1 with Trip Indicator

A Appendix

Figure 14-Figure 18 display the interruption of current and the suppression of transient voltages by MOVs in all 5 of the constructed breakers, respectively.

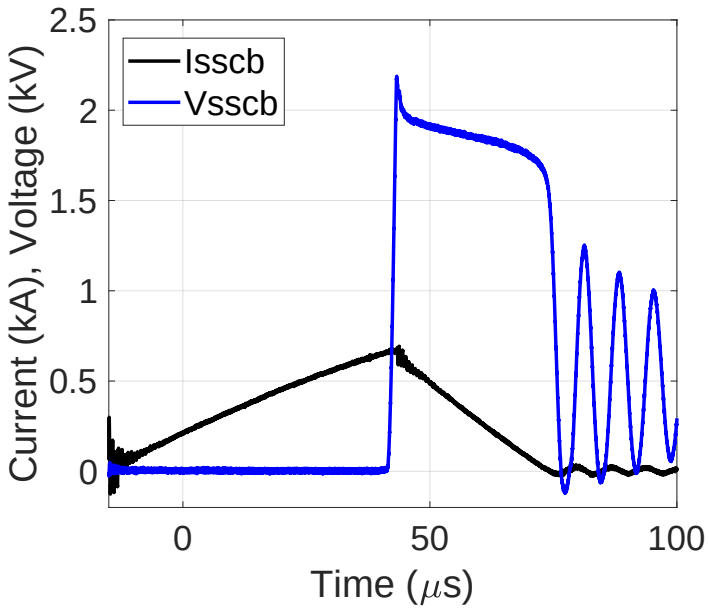

Fig. 14: Current Interruption and Transient Voltages SSCB1

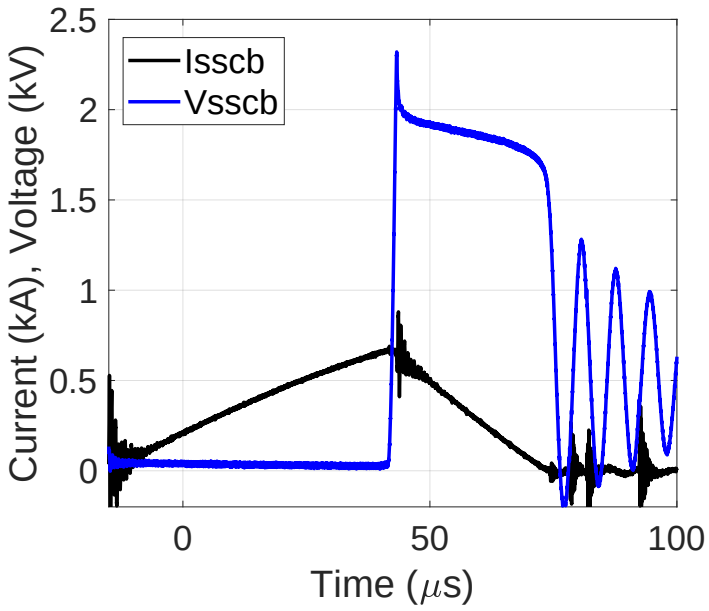

Fig. 15: Current Interruption and Transient Voltages SSCB2

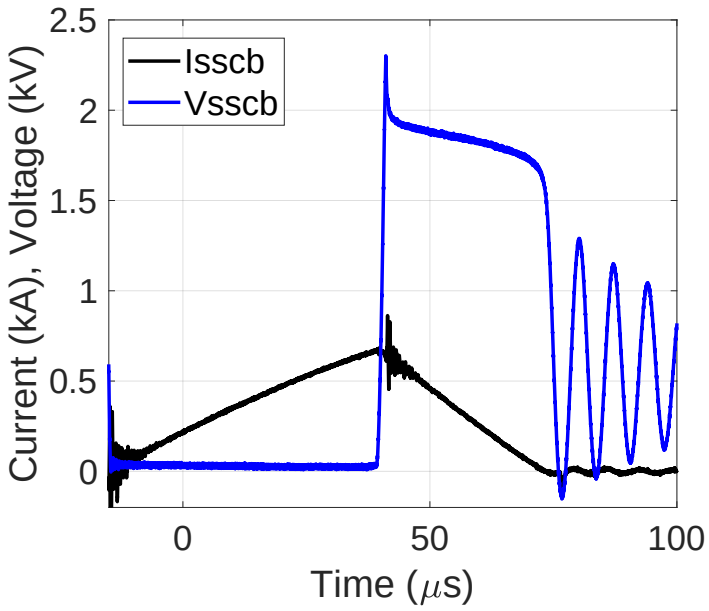

Fig. 16: Current Interruption and Transient Voltages SSCB3

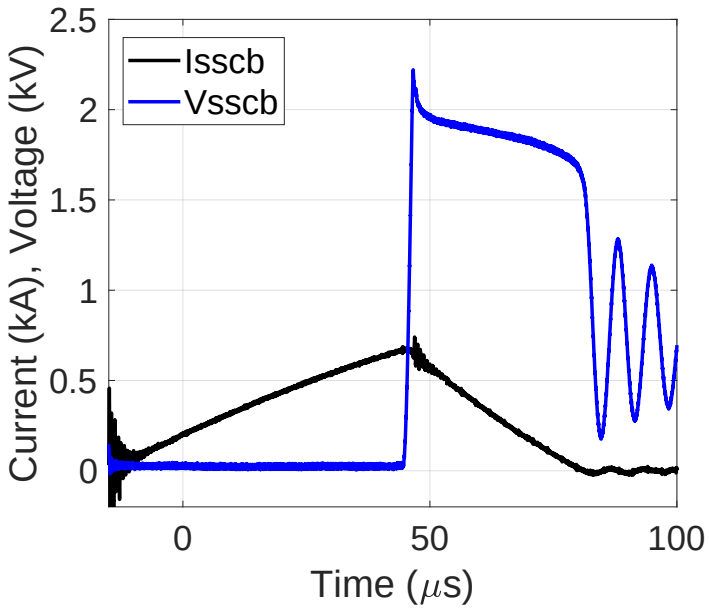

Fig. 17: Current Interruption and Transient Voltages SSCB4

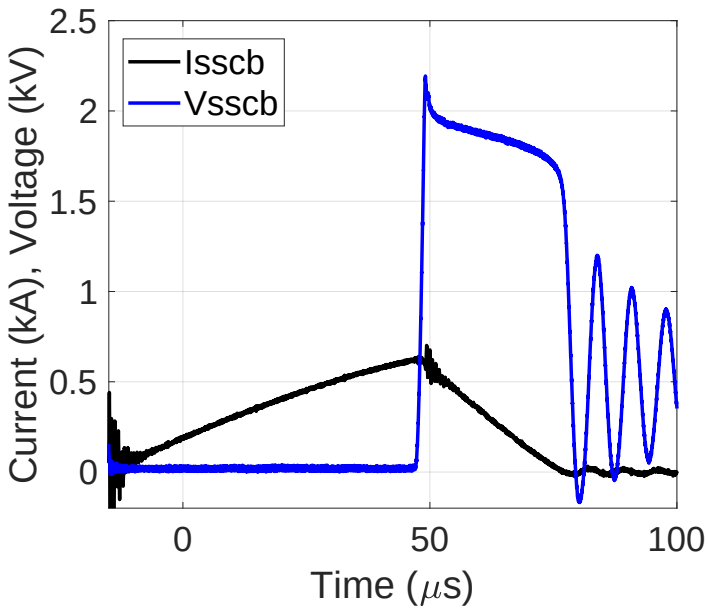

Fig. 18: Current Interruption and Transient Voltages SSCB5